



OVERVIEW OF “PRIMAXX” DRY WAFER CLEANING RESEARCH

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Table of Contents:

* Introduction: Status of Dry Wafer Cleaning Technology	2
* Summary of “Primaxx” Dry Wafer Cleaning Research Activities	3
* Key Results of “Primaxx” Research	4
* “Primaxx Clean” and Its Applications	6
* References: “Primaxx” Literature	9
* Figures Representing Selected Experimental Results (include CONFIDENTIAL information)	12

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Introduction: Status of Dry Wafer Cleaning Technology

During the late '80s gas-phase, or dry, wafer cleaning technology was emerging as a promising solution to some anticipated limitations of wet wafer cleaning methods [1-4]. The research efforts geared toward development of dry cleaning methods initiated at this time did not yield, however, solutions immediately attractive to the industry. This, in conjunction with continuous progress in wet wafer cleaning technology decreased the momentum of dry cleaning research and development. This effort, however, was not abandoned entirely either by researchers (SRC and SubMicron Systems sponsored "Primaxx" research at Penn State, independent "Primaxx" R&D at Lucent-Bell Labs and IMEC, Leuven, Belgium), or by equipment manufacturers (SubMicron Systems, Inc./PRIMAXX) and in some specific areas is bearing now very promising fruits.

The purpose of this Overview is to summarize "Primaxx" dry wafer cleaning research effort. While reviewing this material the following should be kept in mind:

- * After several years of research it has become evident that dry cleaning methods are not meant to replace wet chemistries in mainstream cleaning applications.
- * Performance, clusterability of dry cleans, obvious environmental benefits as well as potentially significant cost of ownership benefits are likely to pave the way for dry cleans into various critical niche applications in IC manufacturing.
- * In these applications, involving both FEOL and BEOL operations, dry surface treatments will be to a larger extent performing surface "conditioning" functions rather than strictly defined surface "cleaning" functions.
- * Dry surface treatments will be implemented primarily in cluster tools rather than in stand alone tool configurations.
- * Besides performance, throughput of gas-phase cleaning modules in the cluster will be a decisive factor for their acceptance.
- * If the cost benefits were to be indisputably proven, then dry cleans will gain acceptance even without having to perform better than their wet counterparts.
- * In some cases availability of gas-phase cleaning chemistries may allow process solutions which otherwise would not be available.
- * As it is demonstrated in this Overview level of performance of gas phase chemistries equal to wet chemistries, or superior, has been accomplished using Primaxx system in some important applications.
- * As of today, "PRIMAXX" is no longer a R&D vehicle, but a fully developed, reliable, six-sided cluster compatible, commercial dry cleaning tool with a set of well defined processes recipes referred to as "**Primaxx clean**".

Summary of “Primaxx” Dry Wafer Cleaning Research Activities

* The gas-phase surface cleaning/conditioning research was initiated at Penn State twelve years ago and involved various aspects of Si surface treatments using gas-phase chemistries (see [5-14]). As a result of a very close collaboration between Penn State researchers and technical staff of Submicron Systems, Inc., a prototype stand alone “Primaxx” dry cleaning module was installed in Penn State’s Microfabrication Laboratory (class100+) in 1992. SubMicron Systems, Inc., providing seed funding for the project and continues to provide limited support for Primaxx project at Penn State until present.

* The schematic diagram of Primaxx reactor as well as chemistries on which research at Penn State is focused are shown in Fig. 1. More detailed technical characteristics of “Primaxx” tool are given in the SMS/Primaxx literature.

* In 1993 the SRC sponsorship of the dry cleaning project using Primaxx tool at Penn State was initiated. This project was terminated after accomplishing its starting objectives in the Fall of 1997.

* Between 1993 and 1995 R&D efforts using the same Priamaxx tool were undertaken at Sharp Microelectronics, Camas, WA, (integrated through Brooks handler with RT gate oxidation module and poly Si CVD module - AGI Integra One), Lucent-Bell Labs, Murray Hill, NJ, (integrated through Brooks handler with RT gate oxidation module), and IMEC, Leuven, Belgium, (integrated through Brooks handler with ASM single wafer epi reactor). Subsequently, “Primaxx” integrated through Brooks handler with RT gate oxidation module and poly Si CVD module (AGI Integra One) was installed in Micron Technology, Boise, ID.

* In parallel, the R&D effort continues in the SubMicron Systems, Inc. demo lab.

* In the Fall of 1997 SEMATECH owned Primaxx module was delivered to Penn State. It is integrated with SubMicron Systems owned Brooks handler and installed in class 10 Nanofabrication Laboratory in Penn State’s Research Park. At this time system is fully plumbed and wired, but due to the delays in the delivery of some key components of the gas delivery system surface cleaning chemistries were not yet run using this system.

* The author of this report spent Fall 97 semester on sabbatical at IMEC, Leuven, Belgium where he conducted research on various aspects of “Primaxx clean”. Selected results of this research presented in this report are marked as *Confidential* as they were not published yet.

Key Results of “Primaxx” Research

This summary lists results of the Primaxx research which were identified by the author of this report as the most important among those to which he had access. It is likely that there were some other important results obtained by researchers working with “Primaxx” which remain confidential.

OVERALL CONCLUSIONS regarding each process investigated.

AHF/methanol

* Based on the results of the anhydrous HF(AHF)/water vapor process and preliminary results obtained by other researchers a low pressure anhydrous HF(AHF)/alcoholic solvent native/chemical oxide etch process was developed at Penn State in collaboration with technical staff of SubMicron Systems, Inc.. Results obtained were published extensively [15-28] and two related patents were obtained [29,30]. Most of the research was focused on AHF/methanol chemistry, but feasibility of other solvents, in particular IPA, was demonstrated. Results of this research were confirmed by other groups working with “Primaxx” tool (e.g. [31,32]).

* Key characteristics of the AHF/methanol etch include:

- Chemical/native oxide can be effectively etched without leaving solid residues on the surface and without adding any particles.
- Etch rates strongly depend on temperature, pressure, and HF partial pressure [15,18,26] (Fig.2).
Typical temperature range: 40 °C - 80 °C; pressure range: 100 torr - 500 torr.
- Etch rates depend on the type of oxide with dry thermal oxide featuring the slowest etch rate and BPSG the highest etch rate [26, 33].
- Si surface following AHF/methanol features higher fluorine coverage (2-3%) than dilute HF (dHF) + Rinse (0-0.5%), and slightly higher than dHF without rinse (1.5-2%) [26,28,31,34]

- Fluorine left on the surface following AHF/methanol treatment is bonded to Si and can not be removed using UV - low pressure treatment. However, it remains on the surface in the doses which are beneficial to the subsequently grown ultra-thin gate oxides.
- Surface fluorine does not affect oxide growth kinetics in the surface reaction controlled oxidation regime (thin and ultra-thin oxides), but slows down oxidation in the diffusion controlled regime (Fig.3),[34-36].
- In “Primaxx” processing concentration of the surface fluorine can be reduced by the subsequent UV/Cl₂ treatment [24, 28] (Fig.4).
- Overall, AHF/methanol etch is a fully developed and well understood process with broad range of applications.

UV/Cl₂

* The UV/Cl₂ process involves exposure of Si surface to UV irradiation in the chlorine ambient. This treatment was first considered by researchers at Fujitsu and then was investigated and adopted for inclusion into the Primaxx cleaning scheme by the Penn State/SMS team.

* Key characteristics of the UV/Cl₂ process include:

- UV/Cl₂ process removes metallic contaminants from the Si surface by slightly etching Si substrate (vaporization and “lift off”).
- Silicon etch rate/metal removal increases with wafer temperature.
Typical temperature range: 50 °C - 200 °C, pressure 10 Torr.
- UV/Cl₂ process is very well suited for slight etching of Si, e.g. for the purpose of surface damage control. Etch rates as low as 20 Å/min.
- UV/Cl₂ process leaves weakly bonded chlorine on the surface.
- Efficiency of metal removal using UV/Cl₂ process depends on the type of metal and the way it was introduced to the surface (e.g. from ashed resist, or from liquid chemicals).
- Metals of greatest concern in Si technology can be effectively removed using UV/Cl₂ process (with an exception of Ca removal of which is less effective). Also, starting metal concentrations should not be exceedingly high (>10¹² cm⁻²) [31, 37-40].

- Properly executed Primaxx UV/Cl₂ process not only does not roughen the surface, but may be used to reduce surface microroughness [41].
- If needed, the UV/Cl₂ process can be used to decrease concentration of F on the surface [24,28].
- In general, the UV/Cl₂ process should not be considered as a “heavy duty” cleaning process, but rather as a surface conditioning process.

UV/oxygen

* The UV/O₂ process involves exposure of the wafer to the shortwavelength UV irradiation in the presence of oxygen. This process was first applied in Si device processing at Penn State [5] and then was incorporated into the Primaxx process.

*** Key characteristics of the UV/oxygen**

- The UV/O₂ process is effective in removing residual organic contaminants from the surface.
- In Primaxx sequence it is applied prior to AHF/methanol oxide etch to assure adequate uniformity of the oxide etching process.
- In the Primaxx clean sequence the UV/O₂ process can also be applied at the end of the surface cleaning/conditioning process in the case stable, oxide passivated surface is required prior to the subsequent process (e.g. gate oxidation).
- Oxidizing strength of the UV/O₂ process is not sufficient to effectively oxidized post-RIE polymer or resist.

“PRIMAXX Clean” and its Applications

* “PRIMAXX clean” includes gas-phase surface treatments described in the previous section applied in the sequence which is determined by the requirements of the subsequent step.

Basic sequences in “Primaxx clean” are as follows:

- * UV/O₂
- * UV/O₂ + AHF/methanol
- * UV/O₂ + AHF/methanol + UV/Cl₂
- * UV/O₂ + AHF/methanol + UV/Cl₂ + UV/O₂

Specific Applications

For specific applications of “Primaxx clean” the following sequences were developed.

Pre-Gate Oxidation

- * (Ashed resist) + UV/O₂ + AHF/methanol + UV/Cl₂ + UV/O₂
- * (SC-1) + UV/O₂ + AHF/methanol + UV/Cl₂ + UV/O₂

- “Primaxx clean” applied before gate oxidation was determined to produce high quality ultra-thin gate oxides particularly in terms of Q_{bd} with other key MOS parameters being equivalent to standard wet cleans or better (Fig. 5 - RTO and Fig. 6 vertical furnace oxidation), [26, 32, 41-43]
- The GOI results were reported for Primaxx clean due to the reduction of the surface microroughness as a result of UV/Cl₂ treatment [42] (Fig.7).
- Pre-gate oxidation Primaxx clean was found effective with gate oxides 15 Å thick [44].

Pre-Epitaxial Deposition (Confidential)

- * UV/O₂ + AHF/methanol
- * UV/O₂ + AHF/methanol + UV/Cl₂

- Pre-epi surface treatment with subsequent epitaxial deposition step is, along with pre-metal surface treatment, probably the most obvious and potentially the most important application of “Primaxx clean” .
- Experiments performed at IMEC where “Primaxx” module is integrated with ASM single wafer epi reactor did confirm suitability of “Primaxx clean” for pre-epi surface treatments in epi clusters [45]. As seen in Fig. 8 “Primaxx clean” performed in the epi cluster on the “wafers out of the box” results in epi (800 °C) layers featuring level and distribution of haze identical to that observed on the starting wafers.

Post-RIE Surface Conditioning

- * UV/O₂ + AHF/methanol + UV/Cl₂
- This sequence was found to be very effective in post-RIE (oxide) surface conditioning by allowing: oxidation of residual organics (polymer), etching of chemical oxide, and slight etching of silicon (about 20 Å) carried out in sequence to remove post-RIE damage. Wide range of experimental results is available to support this claim [46-50].

Pre-Metal Deposition

- * UV/O₂ + AHF/methanol
- This sequence was found equally effective as HF/water dip in removing chemical oxide prior to contact metallization. In contrast to HF dip, however, “Primaxx” process can be readily integrated with metal deposition tool.
- It was found [24,28] that moisture physisorbed on the surface of SiO₂ can be readily removed in “Primaxx” by means of UV/reduced pressure exposure. Furthermore, slight etching of SiO₂ (<30Å) removes layer of oxide containing chemisorbed moisture (Fig.9).
- Etching of chemical oxide at the bottom of contact hole can be accompanied in the “Primaxx” by simultaneous slight etching of field oxide (LOCOS, spacer) to removed top layer of oxide containing chemisorbed moisture, as well as poly gate to remove chemical oxide (Fig.9). This treatment, integrated with subsequent metal deposition (Ti or Co), appears to be potentially very attractive in the “salicide” process.

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DRY CLEANING METHODS APPLIED

(EMPHASIS ON PRE-GATE AND PRE-METAL)

- * Organics removal >>> UV/Ozone
- * Oxide etching >>> AHF/methanol
- * Metal removal >>> UV/chlorine

TOOL USED

SubMicron Systems, Inc., *PRIMAXX*
Dry Cleaning System

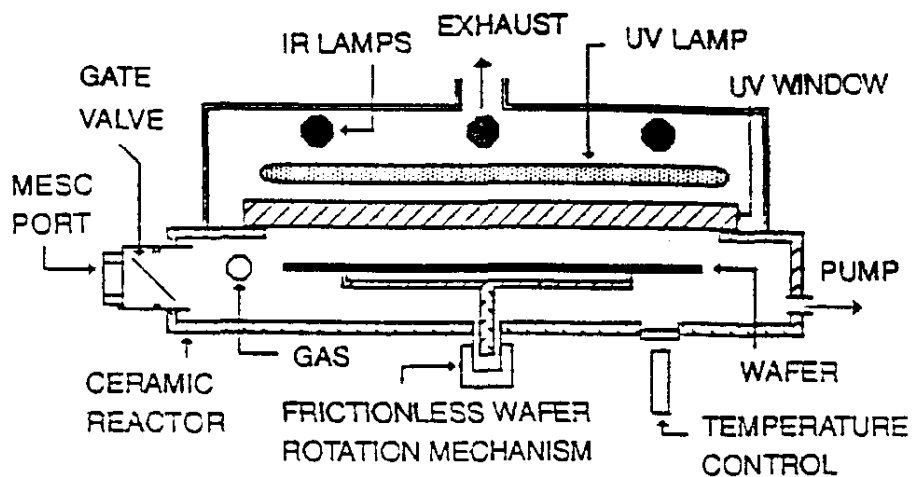


Fig. 1

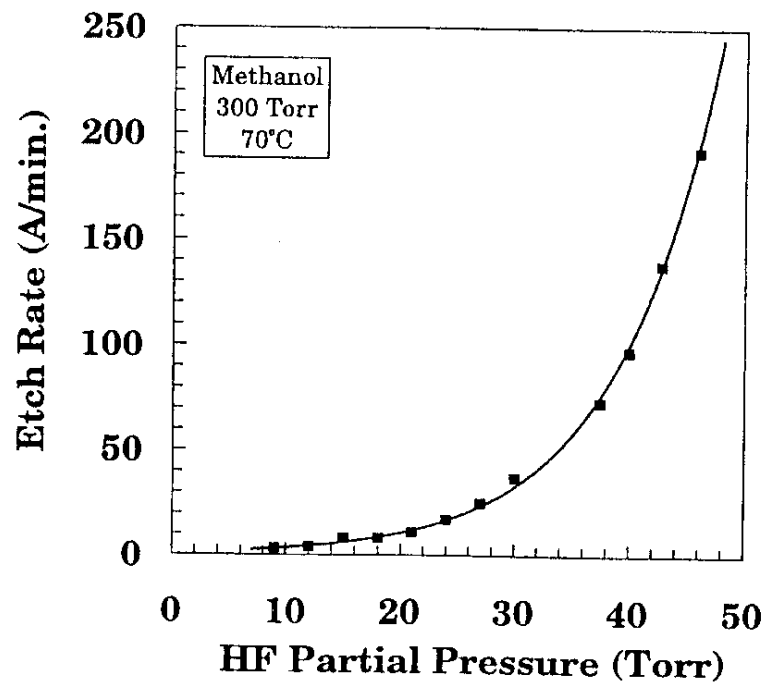
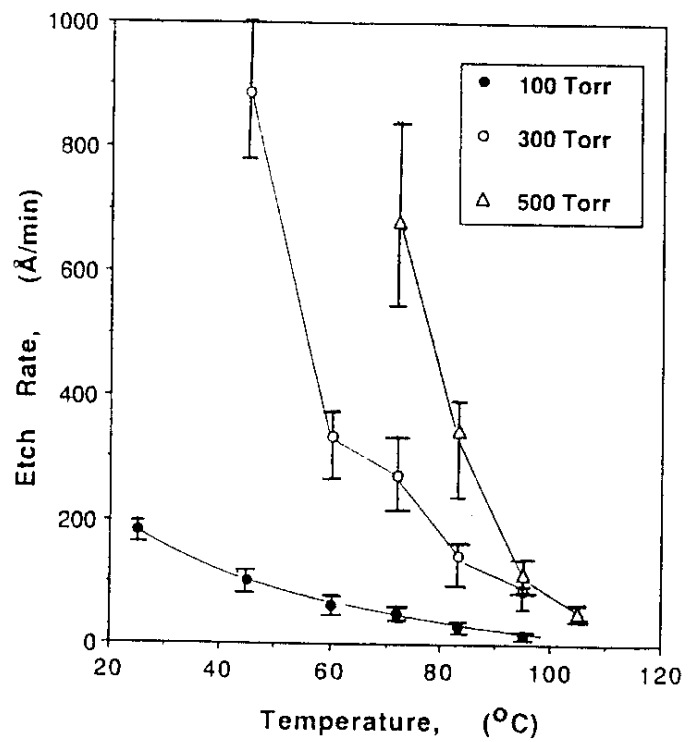


Fig. 2

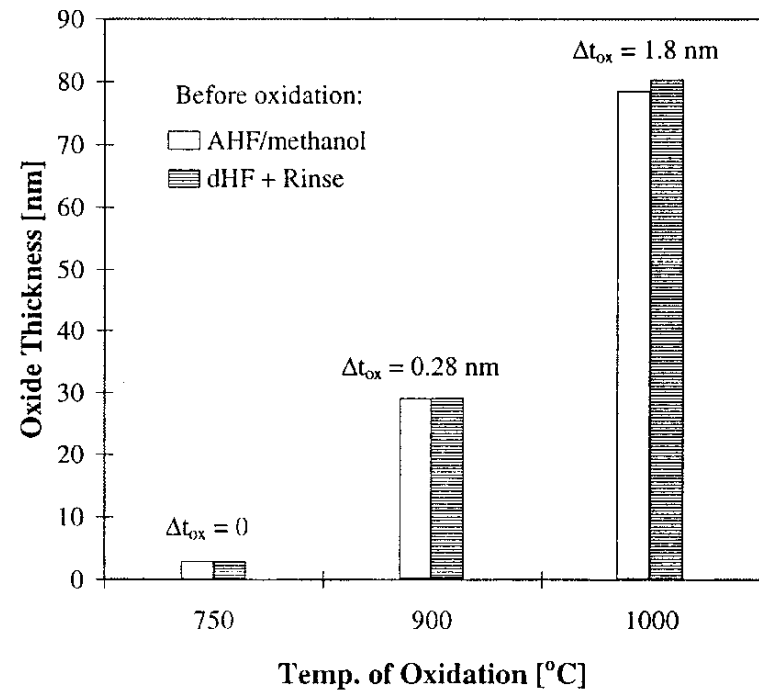
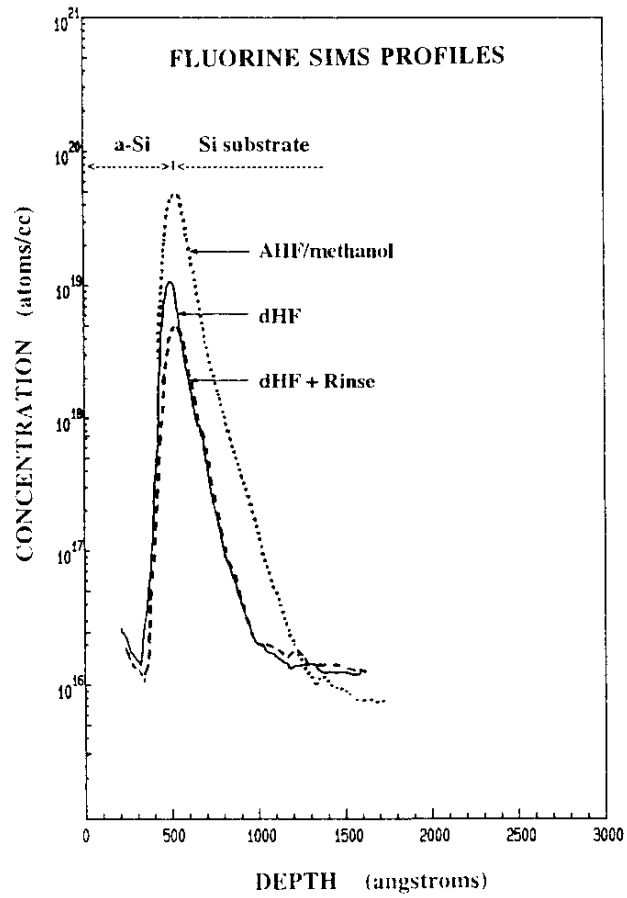


Fig. 3

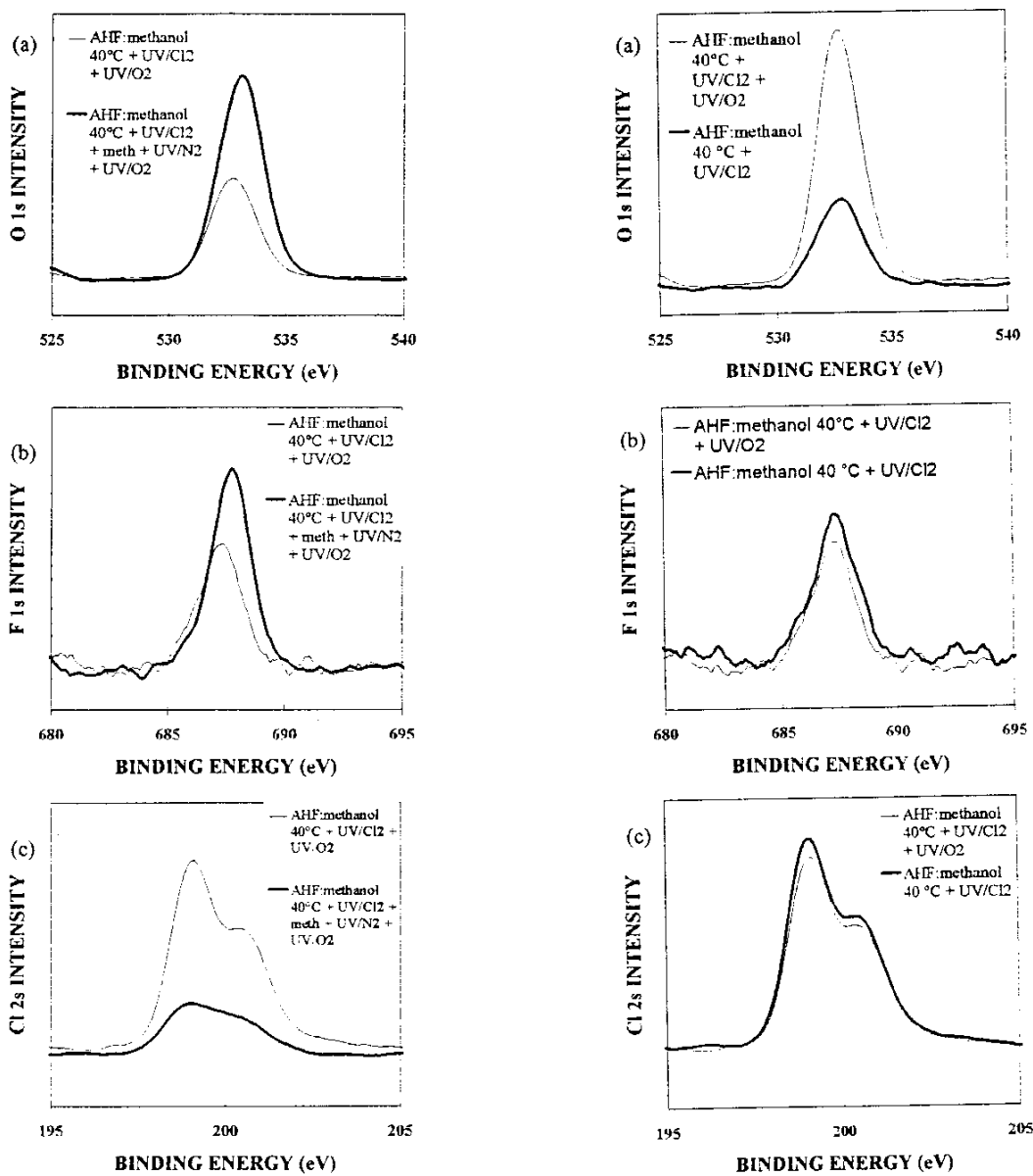


Fig. 4

In Situ Vapor Phase Pregate Oxide Cleaning and Its Effects on Metal-Oxide-Semiconductor Device Characteristics

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Table I. Midgap D_{it} at $\text{SiO}_2/\text{Si}(100)$ interfaces and Q_{bd} of RTO oxides grown on both conventional and *in situ* vapor phase cleaned Si surfaces.

Sample identification	Vapor phase cleaning procedures	Midgap D_{it} ($10^{10}/\text{cm}^2 \text{ eV}$)	Q_{bd} at 50% cumulative failure (C/cm^2)
Control	None	6.2	9.3
A	AHF	5.2	4.8
B	AHF + UV/ Cl_2	8.0	12.5
C	AHF + UV/ O_3	4.2	7.6
D	AHF + UV/ Cl_2 + UV/ O_3	5.7	11.6

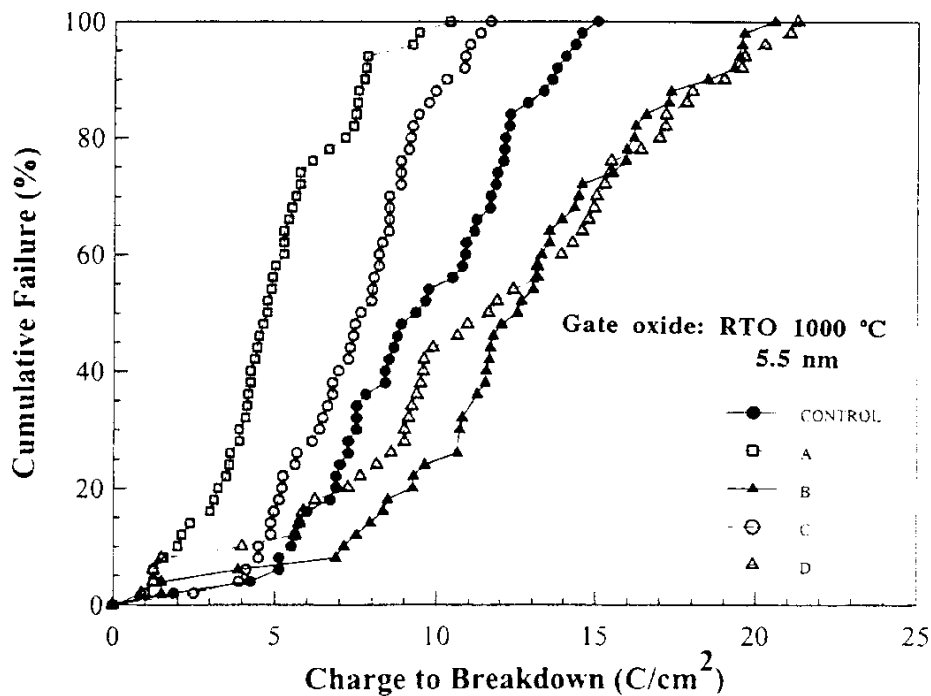
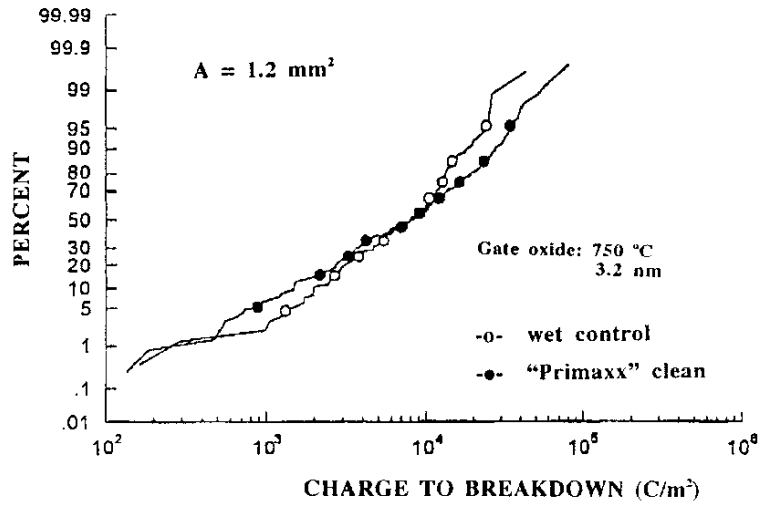
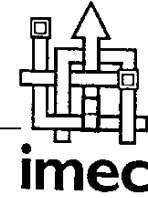


Fig. 5



CONFIDENTIAL

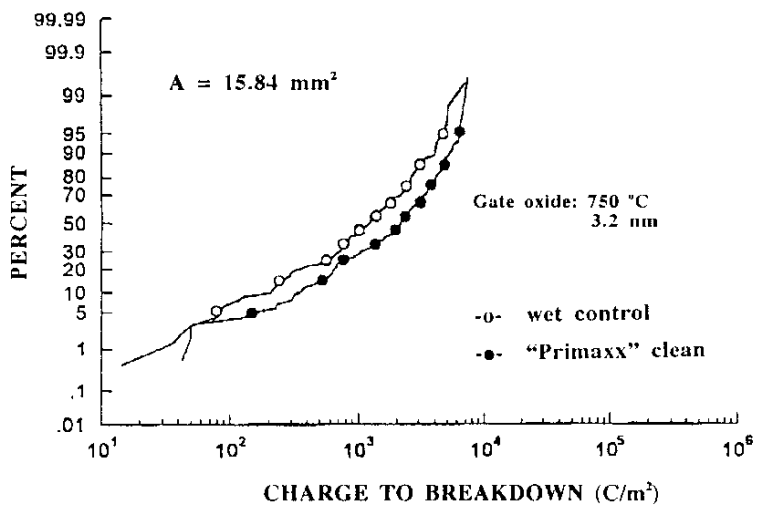
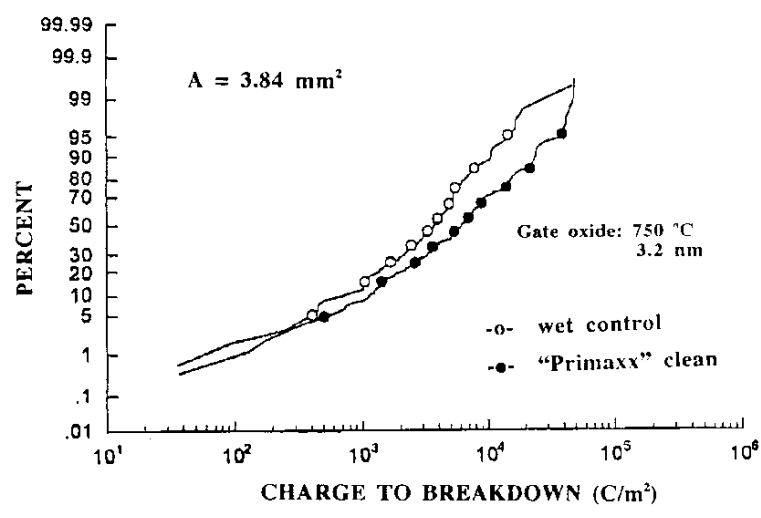
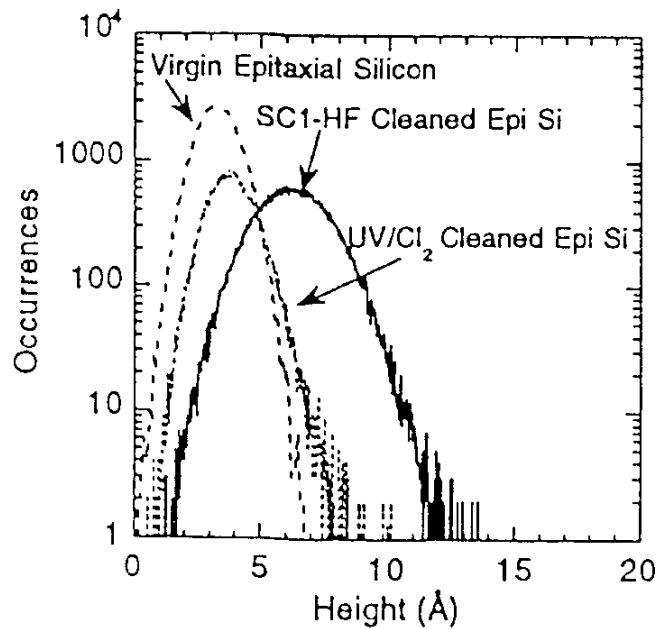


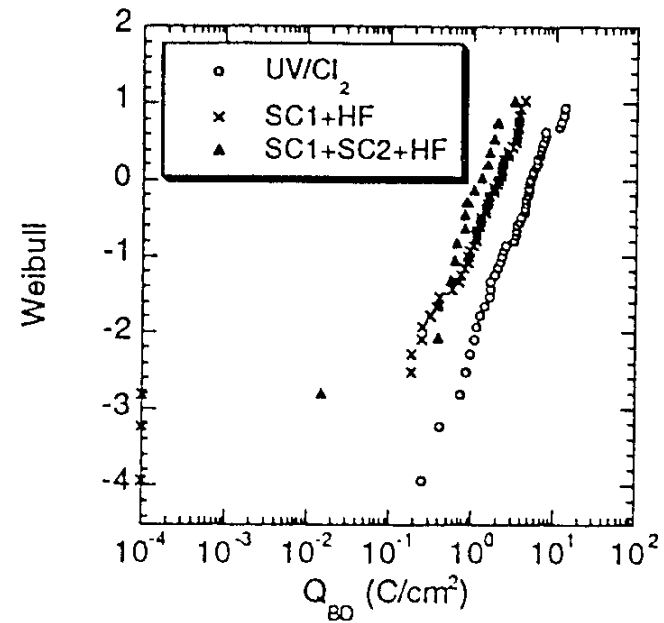
Fig. 6



J. Sapieta, T. Boone, J.M. Rosamilia, P. J. Silverman, T.W. Sorsch, G. Timp, and B.E. Weir, "Minimization of Interfacial Microroughness for 13-60 Å Ultrathin Gate Oxides", Proc. Symp. Sci. and Technol. of Semicon. Surface Prep., Mat. Res. Soc. Proc. Vol 477, (1997), p. 271.



Height distribution of AFM data presented in Figure 1: virgin epitaxial Si (Fig. 1b); SC1-HF cleaned epi Si (Fig. 1c), and UV/Cl₂ processed epi Si (Fig. 1f).



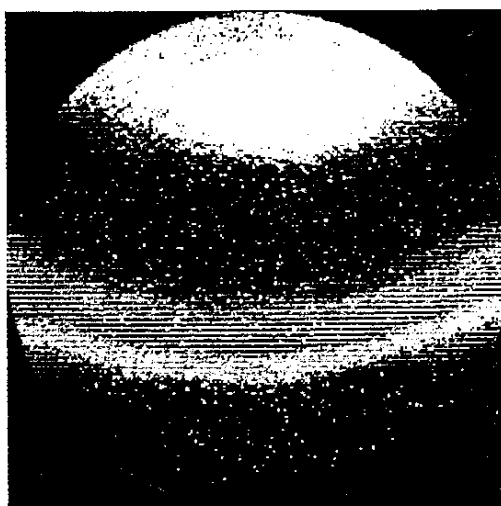
Weibull distribution for 30 Å oxide capacitors, showing the influence of wet and vapor-phase cleans on charge-to-breakdown behavior



CONFIDENTIAL

HAZE MAPS

Wafer out of the box

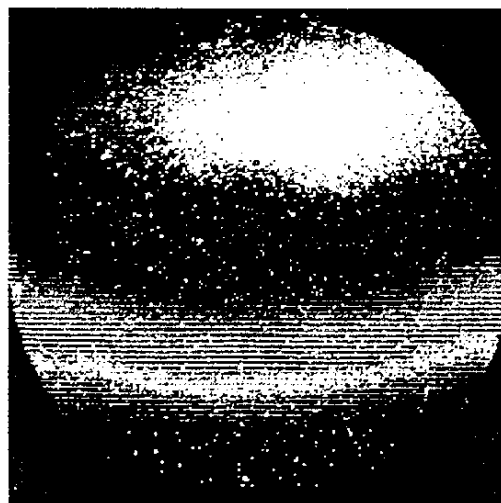


CENSOR ANS

Haze (ppm) 0.097+
Raw LPDs 1220
Reduced 963
Scratches 0
(displayed) 94.0%

(ppm)	(ppm)
2.503	0.112
2.325	0.114
2.146	0.110
1.968	0.107
1.789	0.104
1.611	0.102
1.432	0.099
1.254	0.096
1.075	0.092
0.896	0.089
0.718	0.085
0.539	0.082
0.361	0.078
0.182	0.075
0.000	0.072

“PrimaxxClean” [UV/O₂ + AHF/meth. + UV/Cl₂]
+ Epi deposition



CENSOR ANS

Haze (ppm) 0.104+
Raw LPDs 1157
Reduced 900
Scratches 0
(displayed) 94.2%

(ppm)	(ppm)
2.501	0.117
2.332	0.115
2.153	0.113
1.974	0.110
1.795	0.108
1.615	0.106
1.436	0.103
1.257	0.101
1.078	0.099
0.899	0.096
0.720	0.094
0.541	0.091
0.362	0.089
0.183	0.086
0.000	0.083

Fig. 8

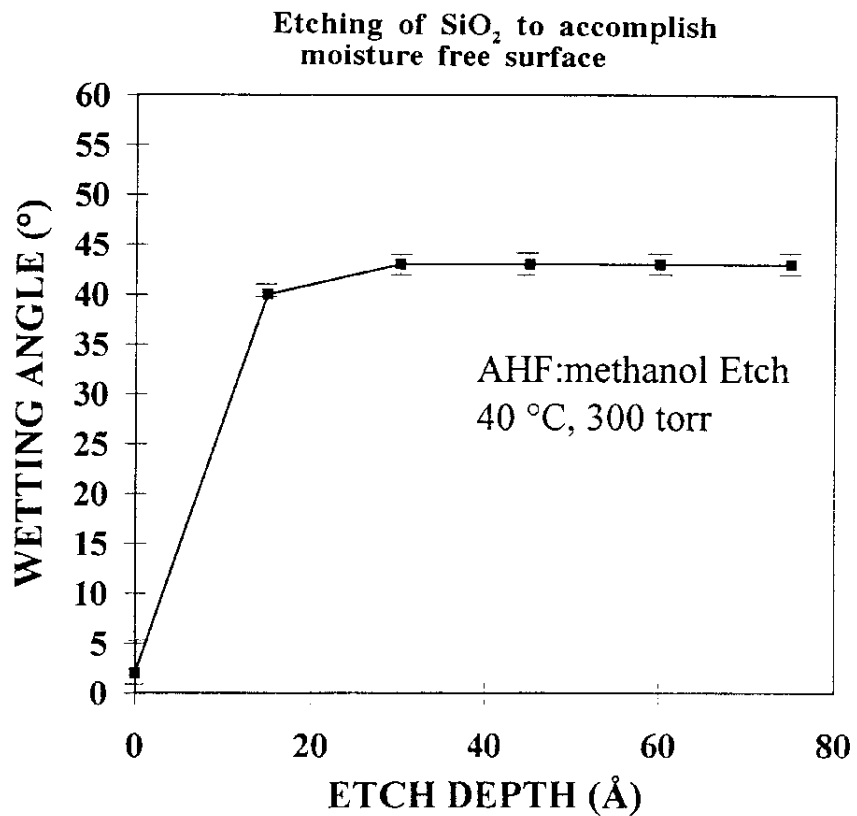
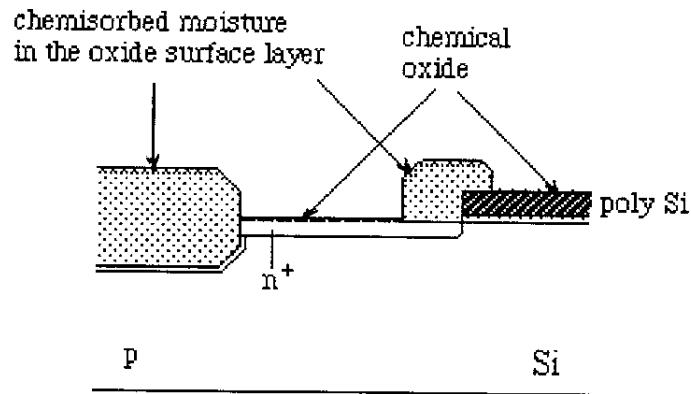


Fig. 9