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On the capacitance of metal/high-*k* dielectric material stack/silicon structures

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Abstract

The accumulation capacitance of metal–insulator–Si capacitors with $SrTa_2O_6$, $ZrSiO_4$-based high-*k* gate dielectrics is observed to have significantly different dependence on the temperature and the frequency of a capacitance–voltage measurement than that of the conventional metal–oxide–Si capacitors. It is shown that this is due to contributions from the, often, inadvertently grown, and relatively poorer quality interfacial dielectric between the high-*k* material stack and the Si substrate.

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1. Introduction

CMOS continuous miniaturization necessitates the use of high dielectric constant (high-*k*) materials to replace thermally grown silicon dioxide as gate dielectrics in the gate stack material systems of MOSFETs. Interfacial layers between the high-*k* dielectric and the silicon substrate are intentionally or unintentionally introduced in the material system. Intentional layers are normally thermal oxides, silicon nitrides, or oxynitrides. Inadvertently formed interfacial layers, however, occur during dielectric deposition stages or during post-deposition annealing in oxygen ambient, and these layers may be composed of low quality nitrided-oxide/oxynitride and metal silicides, depending on the high-*k* dielectric chemistry and growth conditions [1–4]. Because interfacial layers are usually 10–30 Å-thick and have *k* values below 10, they would severely limit the effective oxide thickness (EOT) of the high-*k* gate dielectric [1,2]. Various efforts have been made to reduce the thickness or ultimately eliminate these interfacial layers, however these efforts were mostly unsuccessful [3,5]. In spite of its adverse effects on EOT, some research groups argue that the presence of an interfacial layer may improve the electrical properties of the gate stack system, thereby, justifying the inclusion of the interfacial layer with a controlled thickness. These arguments led to the intentional introduction of the high quality nitride/oxynitride interfacial layer with most efforts focusing on the reduction of its thickness. Nonetheless, reports on the electrical effects of the interfacial layer are very scarce and, in many occasions, highly inconsistent [6,7]. For instance, it has been reported that oxynitride layers formed using NH_3 or NO gases can prevent O_2 diffusion into the Si substrate and subsequent silicon oxide growth. These oxynitride-containing gate stacks are reported to have relatively low interface states and low leakage current. These findings are contrary to other results suggesting that the inclusion of the oxynitride has no obvious effect on the interface quality but it introduces more charge states in the gate dielectric.

In this article, we report on studies of the electrical properties of metal–insulator–Si (MIS) capacitors with high-*k* gate dielectrics. Based on the experimental results and circuit analysis, we argue that the capacitance of the MIS is critically determined by the quality of the

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interfacial layer, perhaps, in a manner that is more subtle than merely the layer thickness. This proposition calls for a more serious consideration of the interfacial layer quality when introduced intentionally and, more importantly, the elimination of any additional low quality layer(s) in the gate dielectric stack. It also calls for careful analysis of the capacitance–voltage (*CV*) results on such MIS capacitors and the use of these results in the estimation of effective *k* values and EOTs for the gate dielectrics.

2. Experimental procedure

p-Type (1 0 0) Si wafers with resistivity of 2–15 Ω cm were used in this experiment. Two types of samples were prepared. The first, referred to as "MOS" (for metal–oxide–Si) capacitor, included a single layer of 20 nm thick oxide thermally grown directly on the n- or p-type Si at 1000 °C and was used as a reference. The second, referred to as "MIS" capacitor included a two-layer gate dielectric: a layer of slightly nitridated oxide formed by UV/NO oxidation carried out at 200 °C after in situ gas-phase Si surface treatments; and a layer of high-*k* dielectric, either $SrTa_2O_6$ or $ZrSiO_4$, formed by means of liquid source misted chemical deposition (LSMCD) in a module integrated with a surface preparation module in a commercial 200 mm cluster [8]. The final thickness of both layers was established in the course of post-deposition anneal carried out at temperatures not exceeding 700 °C and was determined by means of transition electron microscopy (TEM). Under the process conditions applied in this experiment the thickness of the resulting slightly nitridated interfacial SiO_x was in the range of 2.0–2.5 nm while the thickness of high-*k* dielectric varied from 5.0 to 7.5 nm. The MIS capacitors were made only on p-type Si substrates.

In both capacitor types the gate electrodes were made of e-beam evaporated Pt with contact area varied from 1×10^{-4} to 1×10^{-2} cm^2. The electrical characterization of the capacitors included *CV* measurements at the frequencies of 100 kHz and 1 MHz as well as measurements of current density vs. voltage (*J*–*V*) characteristics. In both cases wafer temperature during measurements could be set at any value from 50 to 300 K.

3. Results and discussion

Fig. 1 shows the typical *CV* dependence on temperature measured at 1 MHz for the control silicon dioxide MOS. As the measurement temperature decreases from 300 K down to 50 K the accumulation capacitance in the MOS capacitor on a n-type Si substrate drops from ~250 to 125 pF resulting in a net change of ~50%. In contrast, the dependence of the MIS capacitance on measurement temperature is quite the opposite as seen in Fig. 2. The *CV* measurements of Fig. 2, taken on a MIS capacitor on a p-type Si substrate with $SrTa_2O_6$ as the high-*k*, give an accumulation capacitance of ~400 pF at 300 K, which increases to ~900 pF at 50 K. The per-

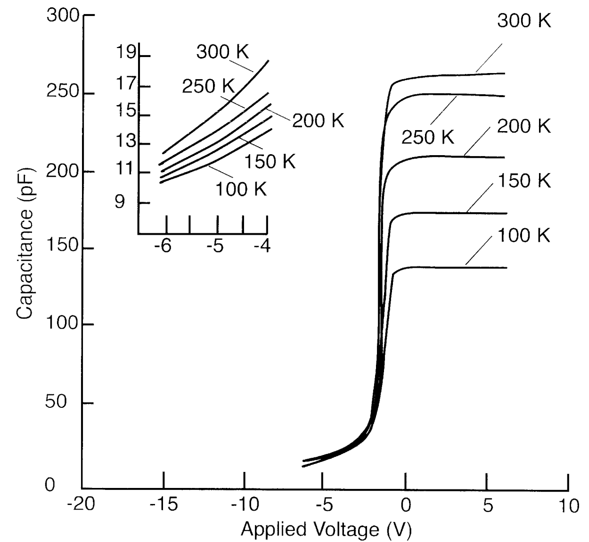

Fig. 1. *CV* curves for 200 Å-thick oxide MOS capacitor SiO_2/Si (n-type Si substrate) capacitor under different *CV* measurement temperatures.

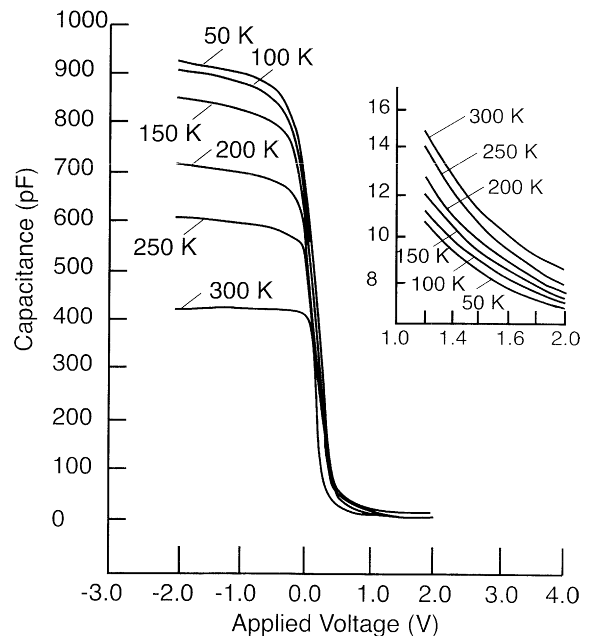

Fig. 2. *CV* curves for $SrTa_2O_6$ MIS capacitor (p-type Si substrate) under different *CV* measurement temperatures.

centage change in the accumulation capacitance of the MIS capacitor is ~125% as the measurement temperature decreases from 300 to 50 K. The dependence of the accumulation capacitance on temperature is much stronger and more pronounced above 150 K. At 100 K and below there appears to be no change in capacitance. However, the deep depletion capacitance in both the MOS and the MIS capacitors (the insets of Figs. 1 and 2) follow similar trends in temperature: the deep depletion capacitance decreases with decreasing temperature. Nonetheless, we note from the slope of the *CV* curves in the depletion region range from 0 to +0.5 V, the *CV* curves measured on the MIS capacitor at higher temperatures tend to be more stretched out indicating more interface state response.

Fig. 3 shows the *CV* characteristics of the MOS and MIS (with $SrTa_2O_6$ for the high-*k* dielectric) capacitors obtained at 300 K and at measurement frequencies of 1 MHz and 100 kHz. The MOS capacitance results in Fig. 3, as well as these shown in Fig. 1, were obtained in structures on n-type Si substrates. However, we reiterate that the observed trends in the capacitance occur in MOS capacitors on both p- and n-type substrates. The MOS accumulation capacitance shows no or very little dependence on the frequency. Meanwhile the MIS capacitance exhibits a rather strong dependence on frequency: the accumulation capacitance more than doubled when the frequency is decreased from 1 MHz to 100 kHz. It is important to point out that the abovementioned dependence on measurement temperature and frequency of the capacitance of the MIS structures is observed irrespective of the high-*k* material in the gate

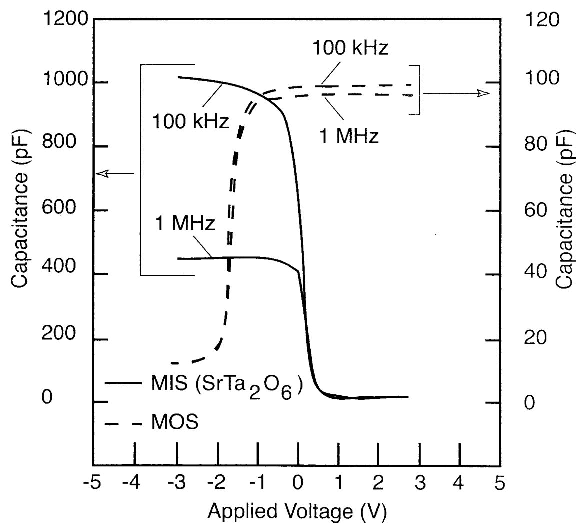

Fig. 3. *CV* curves for both MOS (n-type Si substrate) and $SrTa_2O_6$ MIS capacitors (p-type Si substrate) under different *CV* measurement frequencies (1 MHz and 100 kHz).

dielectric stack. This was observed to be the case for $SrTa_2O_6$, $ZrSiO_4$, HfO_2, and ZrO_2 as the high-*k* dielectrics.

The MOS accumulation capacitance dependence on temperature and frequency can be readily explained by the simple equivalent circuit for the structure, shown in Fig. 4a, where the MOS capacitor in the accumulation region is modeled as a series combination of a capacitor C_{ox}, representing the thermal oxide capacitance, and a resistor R_s which includes Si substrate resistance, as a prime contributor, as well as the back contact and cable resistances. Eq. (1) below relates C_{ox} to the measured capacitance meter output, C_p (Fig. 4a), in accumulation as [9]

$$C_p = \frac{C_{ox}}{1 + \omega^2 R_s^2 C_{ox}^2} \tag{1}$$

where ω is the measurement frequency. It can be seen from Eq. (1) that at 300 K, where for our Si substrate doping $R_s \sim 100\ \Omega$, and at relatively lower frequencies $\omega^2 R_s^2 C_{ox}^2$ ($\sim 10^{-5}$ to 10^{-4}) $\ll 1$ and $C_p \approx C_{ox}$, however a 100-fold increase in $\omega^2 R_s^2 C_{ox}^2$ resulting from a 10-fold increase in ω may cause an insignificant but still measurable decrease in C_p below C_{ox}. We, hence, see the slight decrease (less than 5%) in the accumulation capacitance of the MOS capacitor caused by a frequency increase from 100 kHz to 1 MHz (Fig. 3). Similarly for a given frequency, e.g. 1 MHz, the dependence of C_p on temperature is contained in the substrate resistance R_s which increases by orders of magnitude (two orders of magnitude for our substrate doping level) as the temperature drops from ~300 to ~100 K or below. The change in R_s, in this case, is large enough to make $\omega^2 R_s^2 C_{ox}^2 \sim 1$ below 100 K as opposed to $\omega^2 R_s^2 C_{ox}^2 \ll 1$ at $T = 300$ K. The net effect is the large decrease observed in C_p of the MOS capacitor as the temperature decreases from 300 to 100 K and below (Fig. 1). The above discussion, however, does not explain the much larger change (~100%) in the capacitance of the MIS capacitor as the frequency changes from 100 kHz to 1 MHz and is contradictory to the increase in the MIS capacitance with decreasing temperature (Fig. 2). Therefore this model does not describe the *CV* behavior in the MIS structure.

To explain the behavior of the MIS capacitance, it is necessary to reckon with contributions from the interfacial layer between the high-*k* dielectric and the Si substrate, especially that this layer is, presumably, leaky and of degraded dielectric qualities. Therefore, the equivalent circuit for the MIS capacitor in accumulation is as shown in Fig. 4b. It includes a capacitance C_{HK} which replaces C_{ox} in the earlier model and is contributed by the high-*k* dielectric, an admittance contributed by a leaky interfacial layer, which is a parallel combination of a capacitance C_i and a finite resistance R_i, as

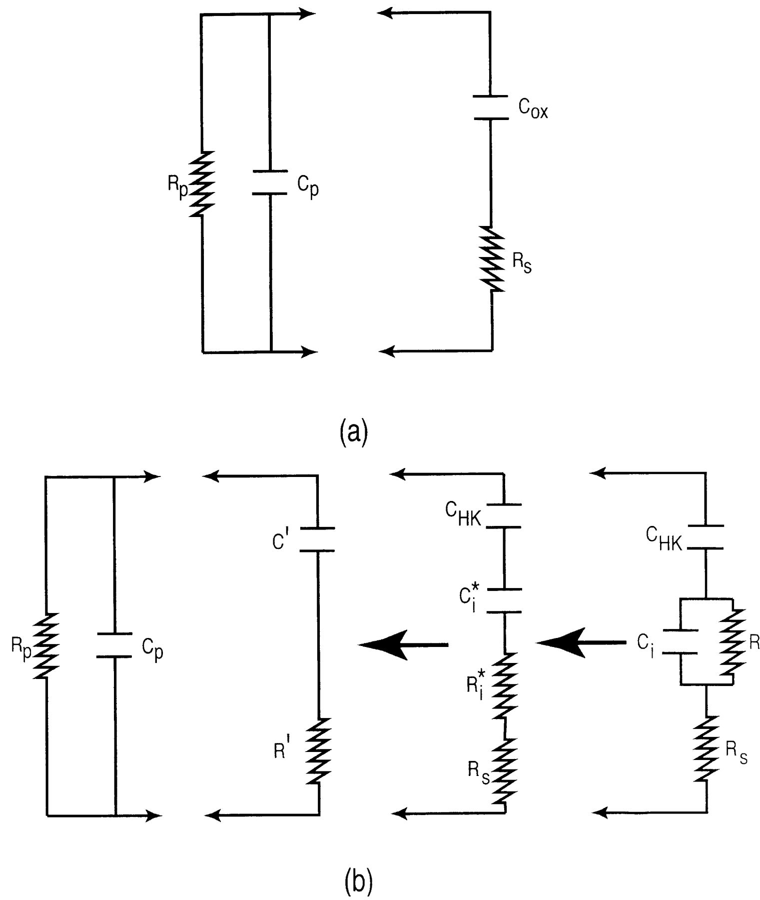

Fig. 4. Equivalent *CV* measurement circuit for (a) MOS capacitor and (b) MIS capacitor.

well as the substrate resistance, R_s. The circuit analysis gives for the measured accumulation capacitance, C_p,

$$C_p = \frac{C'}{1 + \omega^2 R'^2 C'^2} \tag{2}$$

where

$$C' = \frac{C_{HK} C_i^*}{C_{HK} + C_i^*} \text{ and } R' = R_s + R_i^* \tag{3}$$

and

$$C_i^* = \frac{1 + \omega^2 R_i^2 C_i^2}{\omega^2 R_i^2 C_i^2} \text{ and } R_i^* = \frac{R_i}{1 + \omega^2 R_i^2 C_i^2} \tag{4}$$

The conduction in layers of the oxynitride/metal silicide composition types is that of carrier hopping between vacant electronic states in the energy bandgap of the layer. Hopping conduction is enhanced by the concentration of the gap states, however for the same gap state concentration hopping conduction also increases with temperature and the applied voltage frequency [10,11]. At very low temperatures ($\leqslant 100$ K) the hopping conductivity of the interfacial layer is very low and, hence, R_i is large: from Eq. (4), and as R_i becomes large R_i^* becomes small and $C_i^* \to C_i$. Therefore, at the low temperature limit $R' \approx R_s$ and the measured capacitance, C_p, becomes comparable to the series combination of C_{HK} and C_i, i.e., $C_p \approx (C_{HK} C_i)/(C_{HK} + C_i)$.

At high temperatures ($\gg$300 K), on the other hand, R_i is small and so is R_i^* and $R' \approx R_s$, however C_i^* is large and C' approximates C_{HK}. Hence, the measured capacitance at the high temperature limit becomes comparable to the high-*k* dielectric capacitance ($C_p \approx C_{HK}$). It is apparent from the preceding arguments that for both high and low values of R_i, occurring at low and high temperatures, respectively, R_i^* is very small and, accordingly, $R' \approx R_s$ at low and high temperatures. However, from Eq. (4) it can be shown that R_i^* attains a maximum value of $1/(2\omega C_i)(\sim 10^4\ \Omega)$ which occurs at $R_i = 1/(\omega C_i)(\sim 10^4\ \Omega)$. This value for R_i is typical for lossy dielectrics at intermediate temperatures in the neighborhood of 300 K. At these intermediate temper-

atures, $R' \approx R_i^* \approx 1/(2\omega C_i)$ causes $\omega^2 R'^2 C'^2 \sim 1$ in the denominator of Eq. (2) and thereby causes the value of the measured capacitance, C_p, to drop.

In the preceding discussion it is assumed that C_{HK} is not significantly changed within the somewhat narrow temperature range (50–300 K) of these experiments; the implication is that k remains constant. We could not find any reports in the literature for the temperature dependence of k in the high-k dielectrics used in these studies. Nonetheless, k for similar dielectrics, such as Al_2O_3, SrZrO, $Ln_2Ti_2O_7$, are reported to increase with decreasing temperature. However, this increase occurs only at very high frequencies in the GHz range and even then, this increase is reported to be less than 10% within the range 300–50 K [12].

We now turn our attention to the accumulation capacitance dependence on ω for a given temperature. This dependence is contained in the second term $\omega^2 R'^2 C'^2$ in the denominator of Eq. (2). R_i decreases with frequency as the hopping conductance in the interfacial layer increases with frequency. It is predicted that the dependence of hopping conductance on frequency is of the form ω^n where $0 < n < 1$ [10,11]: this causes a $\omega^{2(1-n)}$ power increase with frequency for $\omega^2 R'^2 C'^2$ in the denominator of Eq. (2). The net effect will be the observed decrease in the accumulation capacitance with the measurement frequency as we observed in Fig. 3.

4. Conclusion

It is observed that the accumulation capacitance of MIS structures with high-k gate dielectrics has a strong dependence on the CV measurement temperature and frequency. This is explained as arising from impedance contributions from a low quality interfacial layer between the high-k dielectric and the Si substrate. The fact that the presence of this layer is observed to lower room temperature accumulation capacitance of the MIS structure necessitates that efforts must be put towards its elimination in the gate dielectric stack. Moreover, the presence of this layer must be reckoned with in determining EOT in the MIS.

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