Studies of Mist Deposited High-k Dielectrics for MOS Gates

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Abstract

This paper presents the results of the characterization of high-k dielectric films deposited by Liquid Source Misted Chemical Deposition (LSMCD) in a cluster tool for advanced MOS gates. Electrical characterization (capacitance-voltage and current-voltage) was performed in conjunction with Atomic Force Microscopy (AFM). The effects of *in situ* surface conditioning prior to deposition were also examined. Among processes investigated, the sequence depositing high-k dielectric, e.g. $SrTa_2O_6$ on nitrided oxide interlayer grown by a UV/NO process showed very good promise.

Keywords: high-k; LSMCD; alternate gate dielectric; gas phase clean

1. Introduction

In order to assure the required capacitance of the MOS gate stack in devices featuring geometries below 0.1 μm an extensive search for dielectrics with dielectric constant k higher than that of SiO_2 (3.9) and other characteristics meeting the stringent requirements of MOS gates is currently underway. Among several compositions considered of prime interest are those which feature k higher than 15, are thermodynamically stable with silicon, can be obtained as low-leakage films in the 4-5 nm thickness regime, and maintain their structural integrity during post-deposition annealing cycles. A broad range of materials and deposition techniques is being explored to identify those producing gate dielectrics suitable for next generation CMOS devices.

The Liquid Source Misted Chemical Deposition (LSMCD) method has been successfully employed in the deposition of low-k interlayer dielectrics [1] as well as high-k dielectrics for storage capacitors and ferroelectric RAMs (FRAMs) [2]. In this work we investigate electrical and material characteristics of high-k materials for MOS gates deposited using this method. The materials studied include ZrO_2 and HfO_2 as well as $SrTa_2O_6$.

2. Experimental

The LSMCD technique employs liquid metal-organic precursors as a source and deposits a controlled amount of liquid metal oxides in the form of sub-micron mist droplets onto the wafer surface at room temperature and atmospheric pressure [3]. The process is carried out in a nitrogen ambient and a high-

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voltage electrostatic field is used to control the deposition rate. In this study, the deposition runs were carried out in a commercial cluster (Fig.1) consisting of a gas-phase surface conditioning module, a LSMCD module, and a Rapid Thermal Processing (RTP) module in which wafers are annealed after deposition at temperatures not exceeding 700 ^{o}C. P-type, (100) Si wafers 150 mm and 200 mm in diameter were used as substrates. The pre-surface treatments prior to the film deposition used in this investigation were: (1) *ex situ* native oxide etching in diluted HF (dHF) + rinsing in DI water or (2) *in situ* native oxide etching in anhydrous HF (AHF)/Methanol followed by UV/Cl_2 exposure to remove residual fluorine and slight etch of Si and a UV/NO exposure to grow a nitrided oxide interlayer on the Si-surface. Thicknesses of the dielectric films varied from 3.5 to 15 nm and were determined by means of ellipsometry. Atomic Force Microscopy (AFM) was used to monitor surface morphology of the deposited materials. Current-Voltage (J-V) and Capacitance-Voltage (C-V) measurements were carried out on MOS capacitors with e-beam evaporated Pt/Ti and Pt contacts (7.85×10^{-5} and 3×10^{-4} cm^2).

3. Results and Discussion

In this investigation the promising results, EOT (equivalent oxide thickness) < 1.5 nm, and J_g in the mA/cm^2 range were obtained with HfO_2 and ZrO_2, (Fig.2). However, these results were strongly dependent on the process conditions. The AFM characterization did show occasionally distorted surface morphology and localized discontinuity of surface coverage (Fig.3(a-b)). In the case of Zr and Hf oxides and silicates these features were dependent on the concentration of the precursor and pre-deposition surface treatments.

On the other hand, our experiments indicated that in the case of selected ternary compounds surface energy may be more conducive to the formation by misted deposition of a layer featuring physical integrity superior to that of the Zr and Hf oxides in the desired thickness range (Fig. 3(c)). Figures 4 and 5 shows C-V and J-V curves for 5nm thick $SrTa_2O_6$ [4,5] films deposited on dHF + rinse and AHF/Methanol + UV/Cl_2 + UV/NO-treated surfaces, respectively. EOT values around 1nm were obtained in both cases. However, the leakage current density of the UV/NO sample was approximately one order lower than that of the dHF-treated sample. Furthermore, the interface trap density values were significantly lower for the UV/NO sample. These results indicate that the nitrided oxide layer grown by the UV/NO process better passivates traps at the interface and may serve as a layer reducing leakage currents. On the other hand, ultra-thin layers of $SrTa_2O_6$ were found to be less stable as a function of frequency and electric field than HfO_2 and ZrO_2.

4. Summary

Electrical and material characteristics of various high-k dielectrics deposited by Liquid Source Misted Chemical Deposition (LSMCD) for MOS gates are investigated. Under proper process conditions both HfO_2 and ZrO_2 as well as $SrTa_2O_6$ films with adequate electrical and material characteristics can be obtained. Including a UV/NO gas-phase surface treatment prior to deposition results in an improvement in the electrical characteristics of the MOS gate stacks formed.

References

[1] D.-O. Lee, P. Roman, P. Mumbauer, R. Grant, M. Horn and J. Ruzyllo, in *Meeting Abstracts 199th Meeting Electrochem. Soc.*, 2001-1, the Electrochem. Soc., Pennington, NJ, 2001.

[2] N. Solayappan, V. Joshi, A. DeVilbiss, J. Bacon, J. Cuchiaro, L. McMillan and C. Paz de Araujo, in Integrated Ferroelectrics, G.W. Taylor, Ed., Vol. 22, p. 1, Gordon and Breach Sc. Publishers, 1998.
[3] Technical Literature, Primaxx-2F™, Primaxx Inc., Allentown, PA.
[4] K.J. Hubbard and D.G. Schlom. *J. Mater. Res.*, **11**, 2757 (1996).
[5] I. Tanaka, Y. Sato and H. Kojima, *J. Crystal Growth*, **99**, 837 (1990).

Figure Captions

Fig. 1 Schematic diagram of the cluster tool used in this study.
Fig.2 C-V characteristics of MOS capacitors with 9nm thick HfO_2 and ZrO_2.
Fig.3 AFM results for HfO_2 and $SrTa_2O_6$ each about 10nm thick.
Fig.4 C-V characteristics of $SrTa_2O_6$ on dHF and AHF/meth.+UV/Cl_2+UV/NO-treated surfaces.
Fig.5 J-V characteristics of $SrTa_2O_6$ on dHF and AHF/meth.+UV/Cl_2+UV/NO-treated surfaces.

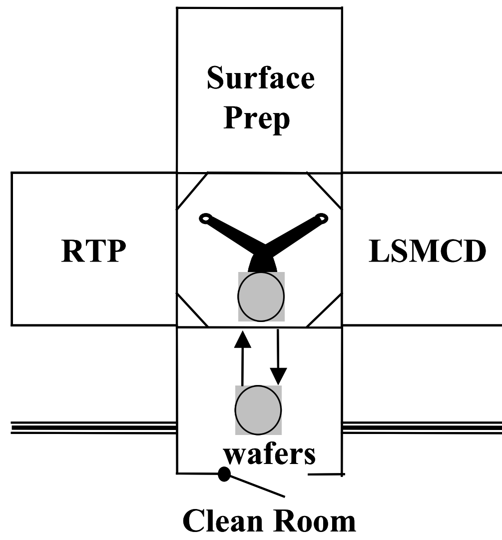
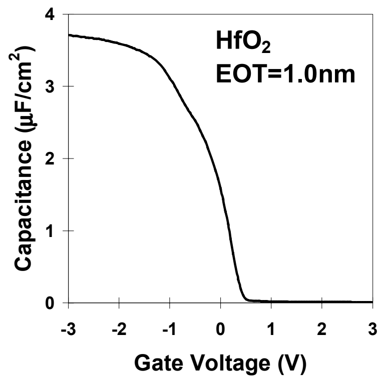


Fig.1



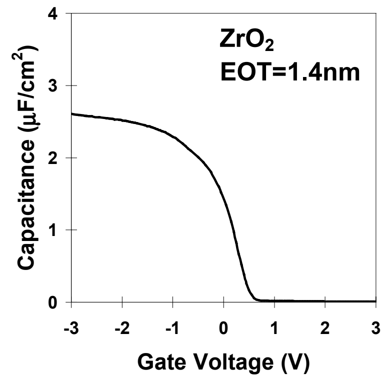
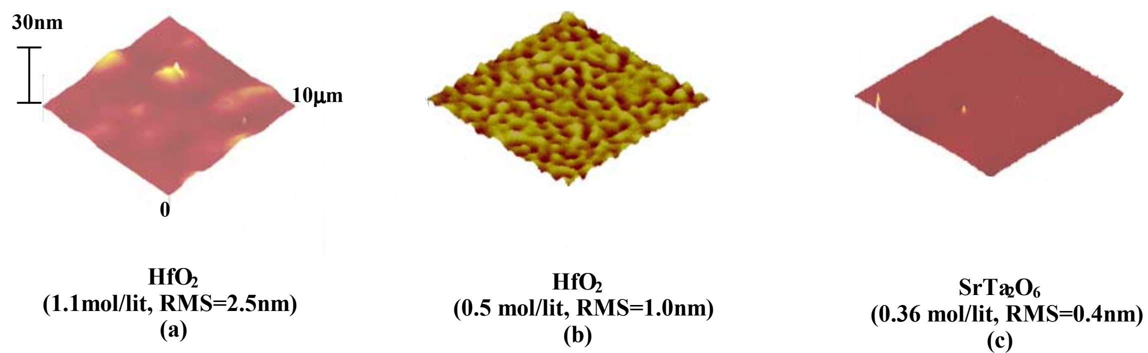


Fig.2

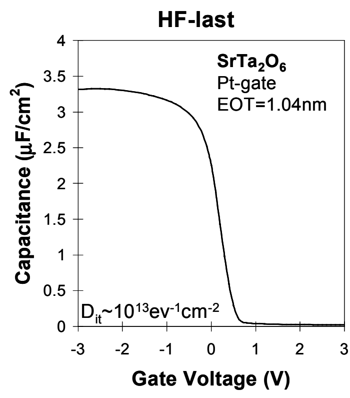


HfO_2 (1.1mol/lit, RMS=2.5nm) (a)

HfO_2 (0.5 mol/lit, RMS=1.0nm) (b)

$SrTa_2O_6$ (0.36 mol/lit, RMS=0.4nm) (c)

Fig.3



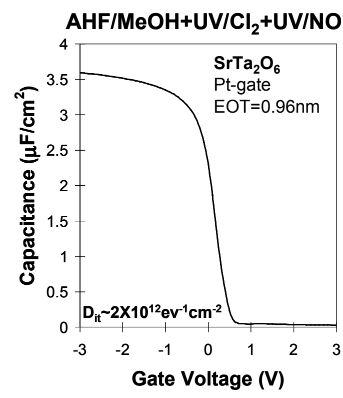


Fig.4

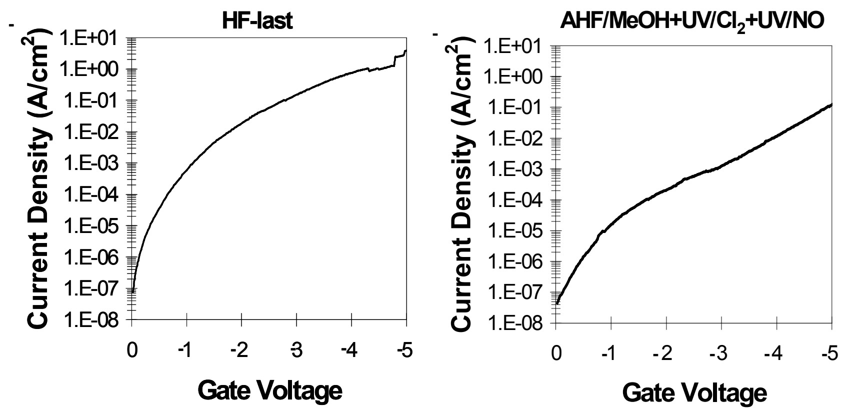


Fig.5