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EFFECT OF THERMAL ANNEAL ON MIST DEPOSITED HFSIO$_4$/SIO$_X$/SI STRUCTURES

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In this experiment mist deposited HfSiO$_4$/SiO$_x$/Si gate stacks are investigated. Following HfSiO$_4$ deposition wafers are subjected to rapid thermal anneals. Time and temperature of these annealing steps define properties of HfSiO$_4$ and thickness of an interfacial SiO$_x$. It was determined that spike anneal at 700°C in nitrogen produced the best results from the point of view of EOT and leakage current. Gate stacks featuring EOT in the range of 1.5 nm at gate leakage current below 10^{-2} A/cm^2 were obtained. No crystallization of mist deposited HfSiO$_4$ was observed during post-deposition RT anneals at the temperature below 900°C.

INTRODUCTION

The effect of an interfacial SiO$_x$ in high-k dielectric MOS gate stacks is beneficial on one hand (superior electron mobility in the channel and resulting high drive current) and detrimental on the other (reduction of the capacitance of MOS gate stack). In select low power device applications the benefits of the former outweigh detriments of the latter Hence, interfacial SiO$_x$ is allowable in these cases providing its thickness and composition are such that equivalent oxide thickness (EOT) in the range of 1.5 nm is obtained at the reduced, comparing to SiO$_2$, limited gate leakage current. Therefore, understanding of the effects controlling formation and properties of ultra-thin interfacial SiO$_x$ in high-k MOS gate structures continues to be in the center of attention in the process of introducing high-k gate dielectrics into mainstream Si manufacturing.

In this work high-k dielectric gate stack formed on Si substrate by mist deposition of HfSiO$_4$ is investigated. In the process of mist HfSiO$_4$ formation, which requires post-deposition anneal, some interfacial SiO$_x$ film is inevitably grown. Thickness and composition of this oxide to a significant degree determines final characteristics of the gate stack. The focus of this investigation is on the interactions of mist deposited HfSiO$_4$ with the underlying Si in the course of post-deposition rapid thermal anneals. Hafnium silicate was selected for this investigation because Hf(O,SiO) compounds appear to show the best promise for replacing SiO$_2$ as a gate dielectric in next generation CMOS ICs, e.g. [1,2]. The mist deposition method was previously used to deposit ferroelectric films

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[3] and also ultra-thin $SrTa_2O_6$ films for MOS gates [4]. In this work it is used to investigate $HfSiO_4/SiO_x/Si$ structures.

EXPERIMENTAL

The method of mist deposition is carried out using process of Liquid Source Misted Chemical Deposition (LSMCD) implemented in a commercial 200 mm compatible module installed on a cluster [5]. In mist deposition (Fig. 1) liquid source material is pushed by nitrogen into an atomizer. In the atomizer liquid is converted into a very fine mist which is then carried by nitrogen to the deposition chamber where it coalesces on the surface of a slowly (10 rpm) rotating wafer at room temperature and pressure very close to atmospheric. In order to control deposition rate beyond gravitational interactions, which in the case of sub-micron sized droplets are very weak, an electric field is created between the grounded field screen and a wafer. After the deposition wafer is transferred by the robot to the RTP module installed on the same cluster (Fig. 2) for a low, typically not exceeding 250°C, temperature anneal in O_2 at atmospheric pressure carried out to solidify the film. Subsequently, wafers are subjected to an additional anneal in the same RTP module at the temperature ranging from 600 °C to 800 °C in pure nitrogen at atmospheric pressure.

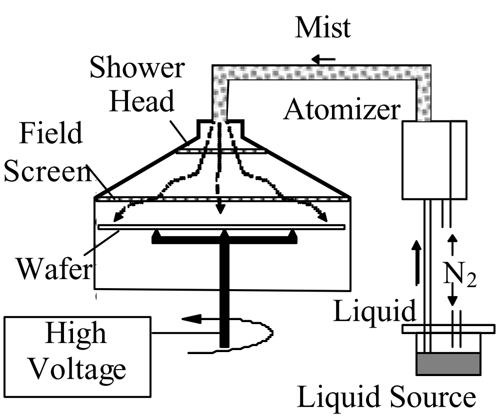

Fig. 1. Schematic diagram of mist deposition module.

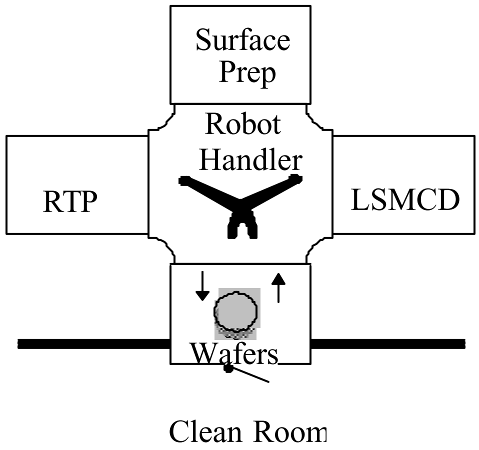

Fig. 2. Configuration of cluster used in this study.

As shown in Fig. 2 cluster used is also equipped with surface preparation module capable of implementing UV/O_2, UV/NO and UV/Cl_2 processes as well as anhydrous HF/methanol (AHF/methanol) etching of native/chemical oxide.

In this experiment ultra-thin (<8 nm) films of $HfSiO_4$ were mist deposited from a liquid source with 1:1 ratio of Hf and Si on oxide-free (HF-last process) or UV/NO treated [6] Si surfaces. In the majority of the experimental runs target thickness of $HfSiO_4$ was about 5 nm. Wafers used were 150 mm, p-type, (100) with resistivity from 1-5 O-cm. For electrical characterization circular Pt gate contacts (1.13×10^{-4} cm^2) were sputtered on the front surface while back surface was metallized with thermally evaporated Al. Film thickness was measured using an ellipsometer and on select samples also using cross-sectional Transmission Electron Microscope (TEM). Other characterization methods used included X-Ray Photoelectron Spectroscopy (XPS) and Atomic Force Microscopy (AFM).

RESULTS AND DISCUSSION

During first stage of this experiment wafers spike-annealed after deposition at 700 ^{o}C were investigated. Based on C-V and I-V measurements of processed devices a plot of density of leakage current J (at -1V on the gate) vs. equivalent oxide thickness was constructed. As seen in Fig.3 results obtained fall in between J-EOT relationships for SiO_2 and HfO_2. This result is as expected for $HFSiO_4$ films, and as such, demonstrates adequate electrical integrity of gate dielectric structure formed by mist deposition.

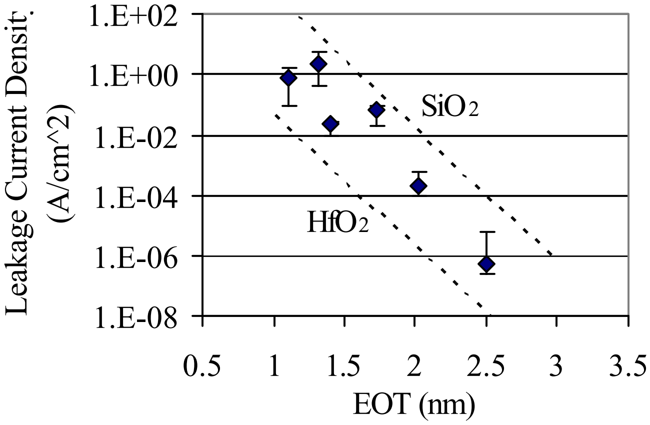

Fig. 3 Leakage current density vs. EOT for SiO_2 [7], HfO_2 [8] (dotted lines) and $HfSiO_4$ in this study.

Analysis of film composition carried out by angle resolved XPS did show approximately 13 at.% of Hf in the film corresponding to Hf/Si^{4+} ratio of roughly 0.7. This is less than theoretical content of 16.7% atomic Hf in $HfSiO_4$ and corresponding Hf/Si^{4+} ratio of 1, and may be taken as an indication of the presence of an interfacial SiO_x-rich oxide buried beneath the $HfSiO_4$ layer. TEM characterization has indeed revealed the presence of an interfacial layer sandwiched in between Si and $HfSiO_4$ (Fig. 4). Thickness of this interfacial film, presumed to be SiO_x, was in the range of 2.2-3.0 nm and was found mostly independent of the thickness of $HfSiO_4$, but dependent on the pre-deposition surface treatments [6], and even more so, on the temperature and time of post-deposition annealing sequence. To determine chemical composition of this film the layer of $HfSiO_4$ was etched off in a weak solution of HF taking advantage of etch selectivity between mist deposited $HfSiO_4$ and interfacial oxide (to be discussed elsewhere [9]). Subsequently performed XPS analysis did show composition of interfacial oxide to be that of SiO_x with only about 0.7 at.% Hf penetration of its uppermost part. This concentration of Hf in SiO_x remaining after etching is not enough to justify significant shift of EOT values in Fig. 3 away from SiO_2 and in the direction of HfO_2. Consequently, it was assumed that additional Hf in the transition region between $HfSiO_4$ and SiO_x responsible for the reduction of EOT was removed during etching of $HfSiO_4$. Although TEM picture shown in Fig. 4 does not allow distinction between pure SiO_2 and Hf containing SiO_x, based on the angle resolved XPS analysis it is postulated that in the case considered thickness of SiO_2 film on the Si surface is roughly 1.2 nm while remaining portion of the transition to $HfSiO_4$ comprises of silicon suboxides with some Hf-O bonds. This assessment remains in agreement with conclusion resulting from the analysis of thermal behavior of ALD deposited $HfSiO_4$ [10]. Furthermore, in spite of the possible catalytic oxidation effect enhancing growth of interfacial oxide in $HfSiO_4$ environment [11] growth of stoichiometric SiO_2 thicker than 2 nm during spike-anneals in N_2 at 700 ^oC is rather unlikely. Hence, it is postulated that in the case of specific process of interest in this experiment a dielectric structure consists of about 1.2 nm thick layer of SiO_2 grown during post-deposition anneal on the Si surface on top of which there is approximately 0.8-1.0 nm thick layer of SiO_x with some Hf-O bonds on which approximately 2.5 nm thick $HfSiO_4$ is located.

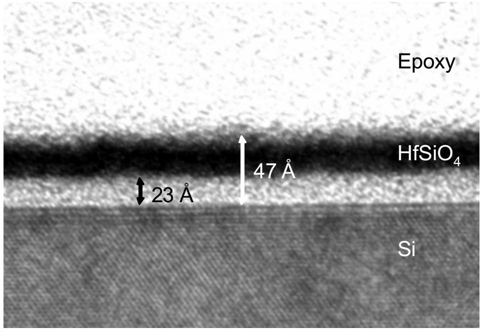

Fig. 4 Cross sectional TEM of $HfSiO_4$ thin film deposited on gas-phase surface treated Si surface.

It should be understood that the numbers quoted above are an estimate only and they may change significantly depending on the conditions of the process - mainly conditions of the post-deposition anneal sequence. In order to better understand the effect of post-deposition anneal on the properties of mist deposited $HfSiO_4/SiO_x/Si$ stack an additional investigation of the effect of post-deposition thermal treatments was undertaken. To determine the process window mist deposited 80 nm thick films of $HfSiO_4$ were subjected to RT anneals and then characterized by X-Ray diffraction spectroscopy (XRD). The results shown in Fig. 5 demonstrate that RT anneals carried out for up to 20 seconds at 1000 ^oC does not seem to affect structure of the film. The indication of phase transformation in the film is observed only after 30 seconds long anneal at 1000 ^oC. Consequently, it was assumed that brief anneals in the temperature range from 600 ^oC to 800 ^oC that are needed to fully develop mist deposited $HfSiO_4$ should not affect structural integrity of the film.

In an early stage of this experiment it was determined that furnace anneal did not allow adequate control over the interfacial oxide growth resulting in too large EOT of the stack. Hence, our attention turned to RT annealing possible with RTP module installed on the cluster used in this study (Fig. 2). To limit thermal budget at any given temperature spike annealing was applied. The best results were obtained when the wafer remained at peak temperature for time t=0. Anneals in which peak temperature was maintained for 20 seconds did produce inferior results in terms of EOT (Fig. 6).

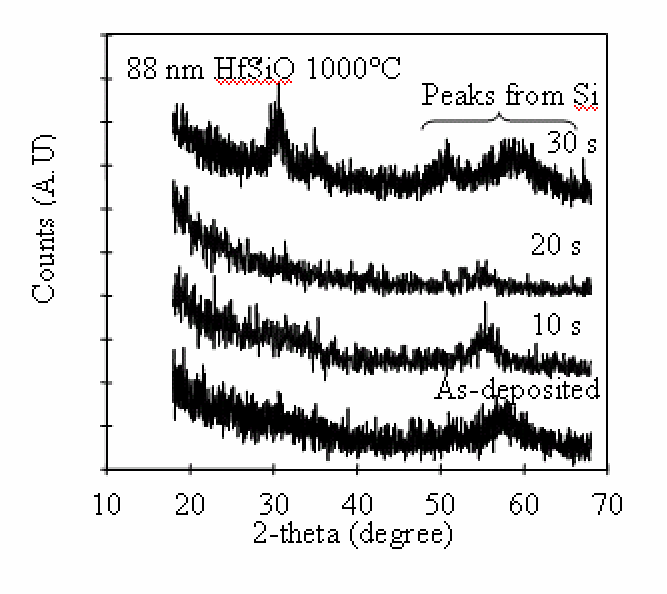

Fig. 5 XRD pattern of 88nm thick $HfSiO_4$ annealed in a RTP chamber at 1000°C in N_2 at different times.

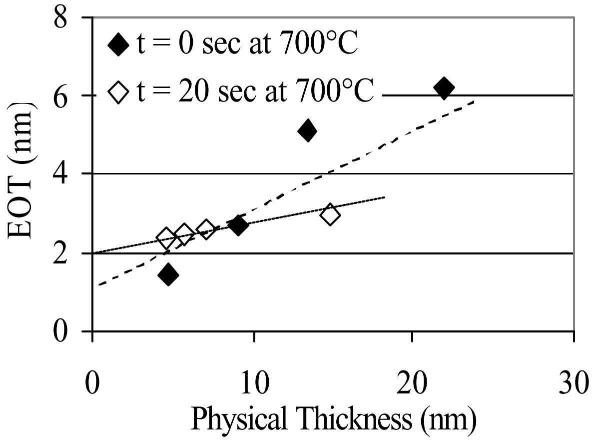

Fig. 6 Physical thickness vs. EOT of $HfSiO_4$ films spike-annealed at 700°C.

The temperature of 700 °C was selected based on investigation of the effect of the temperature of RT annealing on EOT carried out on the wafers with $HfSiO_4$ film in the thickness range from 4.5 to 7nm thick. As expected, with the increase of temperature of anneal EOT increases (Fig. 7) due to increase of the thickness of an interfacial SiO_2. Temperature of 800 °C was found to be too high to control growth of interfacial oxide.

On the other hand, when the anneal temperature was low enough to prevent growth of substantial interfacial oxide then the leakage current was too high (600 °C in Fig.7). The possibility that temperature of anneal may have also an impact of the density of $HfSiO_4$ film itself, and hence electrical characteristics of the stack cannot be entirely neglected. Still, it is rather obvious that the engineering of the interfacial oxide plays a key role in defining MOS gate stacks formed by mist deposition.

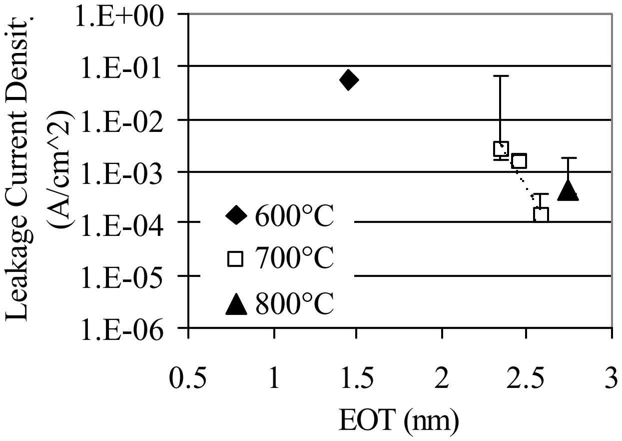

Fig. 7 EOT vs. leakage current density for mist deposited $HfSiO_4$ films spike-annealed at different temperatures.

SUMMARY

This experiment demonstrated that interactions taking palace at the $HfSiO_4/SiO_x$ interface play a key role in defining final electrical characteristics of the gate stack formed by mist deposition. With deposition method and tool used in this study it is expected that the Si-$HfSiO_4$ transition region can be engineered such that EOT of the final gate stack of about 1 nm can be accomplished.

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