

LIQUID SOURCE MISTED CHEMICAL DEPOSITION (LSMCD) OF THIN DIELECTRIC FILMS

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This paper discusses the deposition and characterization of thin dielectric films deposited by liquid source misted chemical deposition (LSMCD) method in a cluster tool. The LSMCD method utilizes an organic based liquid precursor and is effective to deposit ultra thin films up to 4 nm with good conformality and uniformity of deposited films. The C-V and J-V characteristics are investigated for promising high-k dielectrics (HfO_2 , ZrO_2 , and SrTa_2O_6) and EOT (equivalent oxide thickness) 0.9 nm was obtained from 5 nm thick SrTa_2O_6 film. A feasibility work on low-k material (Pyralin PI2610) using LSMCD method is also done and mist deposited low-k film showed excellent electrical characteristics.

INTRODUCTION

Liquid organic precursors are often used as source materials in deposition of thin film dielectrics. Those precursors can be either converted into gas and used in CVD processes or put on the surface of the substrate as a high viscosity liquid using a spin-on process followed by a low temperature anneal resulting in solidification of the film. The advantages of the spin-on process are its simplicity and ability to planarize the surface if needed. Among disadvantages, inherent inability of the spin-on process to cover surface features conformally, significant waste resulting from the fact that only part of the liquid dispensed on the surface forms a thin film, reduced effectiveness in the case of very large diameter wafers, poor film quality and the potential for wafer damage during high rpm spinning should be listed.

A way of covering solid surfaces with liquid dielectric precursors superior to dispensing/spinning liquid on the surface is the method of "misted deposition". As the name indicates, the liquid in this case is slowly delivered to the substrate in the form of a very fine mist which conformally covers surface features. In contrast to spin-on processes misted deposition was demonstrated to allow controlled depositions of dielectric films as thin as 4 nm and as thick as 100 nm. It also uses amounts of liquid significantly lower than spin-on processes to obtain required coverage which reduces overall capital cost and

environmental concerns related to the disposal of organic waste. Moreover, misted deposition is inherently better compatible with large diameter wafers than spin-on processes and does not expose wafers to any mechanical hazards during deposition. Table I compares spin-on to misted-deposition process.

In this study the LSMCD method is investigated as a way to deposit high-k dielectrics (ZrO_2 , HfO_2 , and SrTa_2O_6) for MOS gates and a low-k dielectric (Pyralin® PI2610) for interlayer isolation in multilevel interconnect schemes.

EXPERIMENTAL

Film deposition was carried out in a commercial 4-sided cluster tool as shown in Fig.1. It consists of a wafer handling robot and a radially mounted load lock elevator assembly capable of controlling a single 25-wafer cassette of 150mm or 200mm wafers, a LSMCD module, RTP (Rapid Thermal Processing) module which soft-bakes the wafer at atmospheric pressure below 400°C in either oxygen or nitrogen ambient and a gas-phase cleaning module which performs native oxide etch, silicon surface etch and precleaning of Si wafer surface at a reduced pressure [1]. LSMCD method has been effectively used in depositions of ferroelectric dielectrics (e.g. SBT, PZT) for FRAM applications and high-k dielectrics for storage capacitors. The LSMCD technique employs organic composition chemistries as a source. In the LSMCD system (Fig.2) the liquid is atomized and transferred to the deposition chamber where a controlled amount of dielectric precursor in the form of sub-micron mist droplets is deposited on the wafer at room temperature to form a uniform and conformal coating. The process is carried out in either a nitrogen or oxygen ambient at atmospheric pressure and a high-voltage electrostatic field is used to control the deposition rate. Following deposition wafers are subjected to a low temperature anneal in an integrated low-temperature RTP module. For high-k dielectric depositions the LSMCD cluster is, in addition, equipped with a gas-phase surface preparation module.

P-type 200 mm and 150 mm (100) Si wafers were used as substrates in the high-k gate dielectric work. In situ surface conditioning prior to the high-k film deposition for some runs was done in a gas-phase cleaning module. The presurface treatment in this investigation can be threefold: (1) native oxide etching in diluted HF (dHF) + rinsing in DI water ex situ (2) native oxide etching in anhydrous HF (AHF)/MeOH (methanol) + UV/ Cl_2 exposure in situ for metallic contaminants removal and surface conditioning (3) (2) + UV/NO process in situ to grow NO layer which serves as a blocking layer between silicon surface and high-k gate dielectric materials. The electrical properties of these films were studied via C-V and J-V characterization of MOS capacitors. The diameter of MOS capacitors with e-beam evaporated Pt or Pt/Ti electrodes varied from 0.1mm to 1mm.

For low-k material deposition, p-type 150 mm (100) silicon wafers were used as substrates and metallized with aluminum to provide a bottom electrode. A low-k material Pyralin® PI2610 was 1:8 diluted with NMP (N-methyl-2-pyrrolidone). The low-k material was deposited in LSMCD chamber directly onto the metallized silicon surface. Aluminum front electrodes with 1mm diameter were thermally evaporated through

shadow mask to further construct Metal/Insulator/Metal (Al/low-k/Al) structure for electrical characterization.

RESULTS AND DISCUSSION

During early stage of this work, several compositions were investigated. Among materials investigated, HfO_2 , ZrO_2 and SrTa_2O_6 showed very good performance [2] and we focus on these materials in this paper. Fig.3 (a) shows precursor concentration vs deposition rate at deposition bias voltage 4kV, flow rate 0.15 sccm and deposition time 4 min. The deposition rates linearly increase as precursor concentration increases regardless of the different chemical composition. Deposition rates at different bias voltages (Fig.3 (b)) was also studied for La_2O_3 with deposition time 4 min, flow rate 0.15 sccm, and precursor concentration 0.75 mol/litter. The deposition rate also increases almost linearly as a function of deposition bias voltage.

Fig.4 shows typical C-V curves of mist-deposited ZrO_2 and HfO_2 . At $V_g = -3\text{V}$, capacitance densities of about $2.5 \mu\text{F}/\text{cm}^2$ and $3.3 \mu\text{F}/\text{cm}^2$ for ZrO_2 and HfO_2 , respectively, were obtained. These values correspond to equivalent oxide thickness (EOT) 1.4 nm for ZrO_2 and 1.0nm for HfO_2 . As J-V plots for the same devices shown in Fig.5 indicated, the leakage current density at -1V in either case did not exceed $1\text{mA}/\text{cm}^2$. Unfortunately, these data were not fully reproducible due to incomplete coverage of the films for less than 7nm thick regime and resulting local discontinuity of the films. As opposed to ZrO_2 and HfO_2 , mist-deposited SrTa_2O_6 showed excellent film uniformity and surface roughness in the range of 1nm from AFM. SEM and TEM data also indicated the smooth, complete coverage of the film on the silicon surface. Fig.6 and 7 show C-V and J-V curves of 5nm thick SrTa_2O_6 films deposited on dHF + rinse - treated surface and AHF/MeOH + UV/ Cl_2 + UV/NO -treated surface. The EOT value around 1nm was obtained for both cases. However, the leakage current density of UV/NO -last sample was approximately 1 order lower than that of dHF-last surface. Furthermore, the interface trap density values were significantly lower for UV/NO -last sample. These facts indicate that NO layer grown by UV/NO process may serve as an excellent blocking layer from tunneling currents and from organic contamination.

We also tested the possibility of depositing a low-k material Pyralin® PI2610 manufactured by HD MicrosystemTM using same LSMCD chamber. Fig.8 summarizes J-V, and C-V results which shows a good feasibility of using LSMCD method to deposit low-k materials.

SUMMARY

The fundamental electrical characteristics and material properties of mist-deposited high-k and low-k materials were studied. Among high-k materials studied in this work, SrTa_2O_6 showed very adequate electrical characteristics and material properties which may suggest SrTa_2O_6 as a very good candidate for advanced gate stack application. In addition to high-k work, mist-deposited low-k material also showed excellent electrical properties. In conclusion, LSMCD method offers new possibilities in thin film dielectric processing.

REFERENCES

1. Technical Literature, Primaxx-2F™, Primaxx Inc., Allentown, PA.
2. D.O. Lee, P. Roman, P. Mumbauer, R. Grant, M. Horn and J. Ruzyllo, in *Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues/2000*, M.J. Loboda, R. Singh, S.S. Ang, and H.S. Rathore, Editors, PV 2000-5, p237, The Electrochemical Society Proceedings Series, Pennington, NJ (2000).

Table I Spin-on vs. LSMCD process

Spin-on process	LSMCD process
<ul style="list-style-type: none"> • simple & fast • able to planarize surface • poor conformal coverage • significant chemical waste • poor film quality • problem worse in large diameter substrate 	<ul style="list-style-type: none"> • Cost-effective • Conformal coverage • Better thickness uniformity

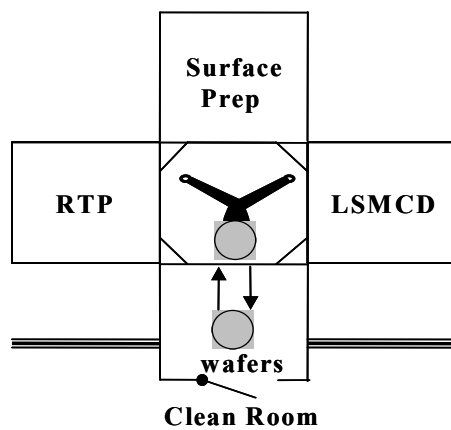


Fig.1 Cluster used in this study

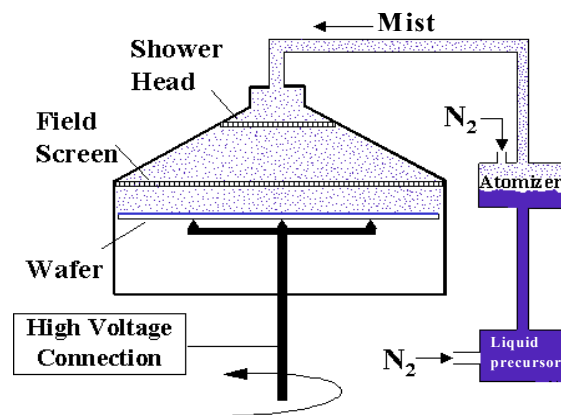


Fig.2 LSMCD reactor schematic

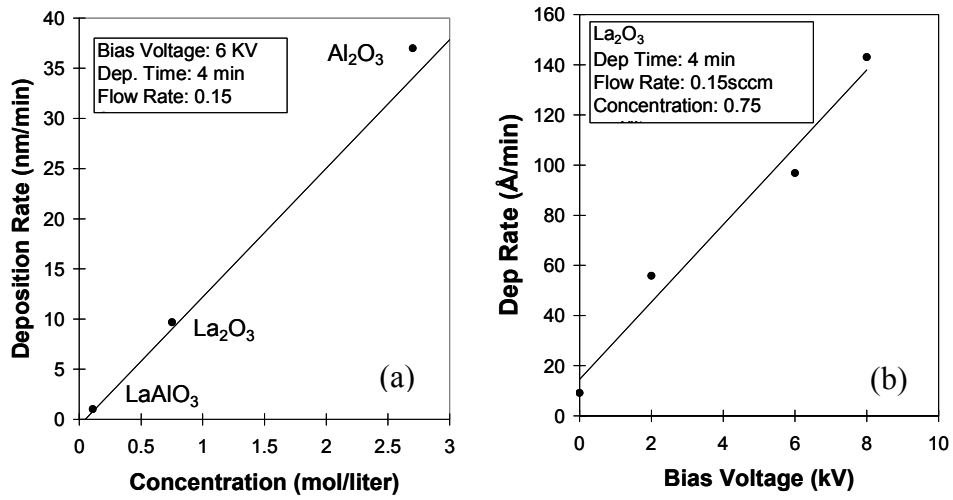


Fig.3 Concentration vs. dep rate and Bias voltage vs. dep rate

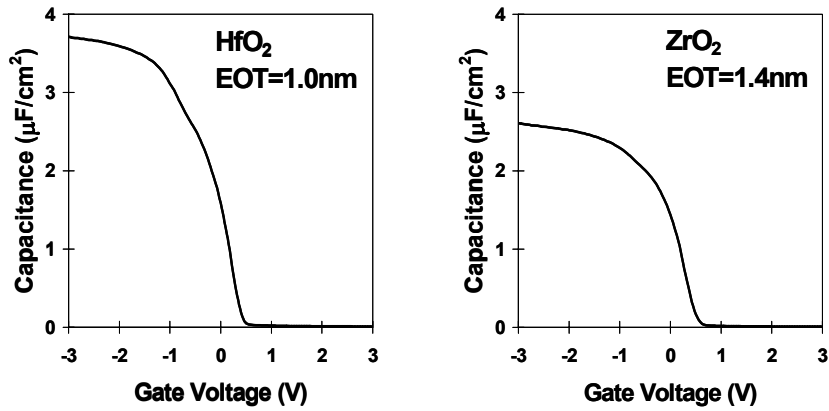


Fig.4 C-V characteristics of 7nm thick HfO_2 and ZrO_2

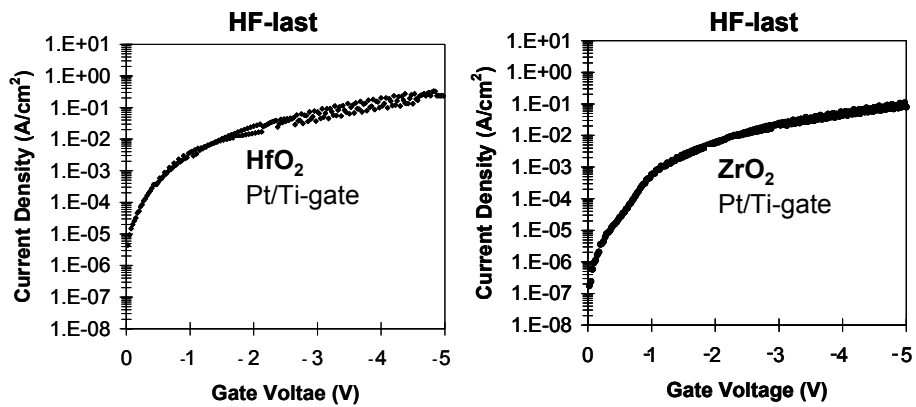


Fig.5 J-V characteristics of 7nm thick HfO_2 and ZrO_2

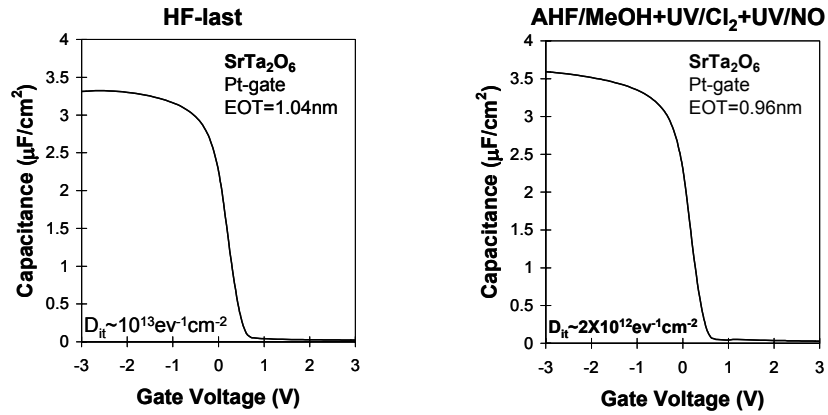


Fig.6 C-V characteristics of 5nm thick SrTa₂O₆

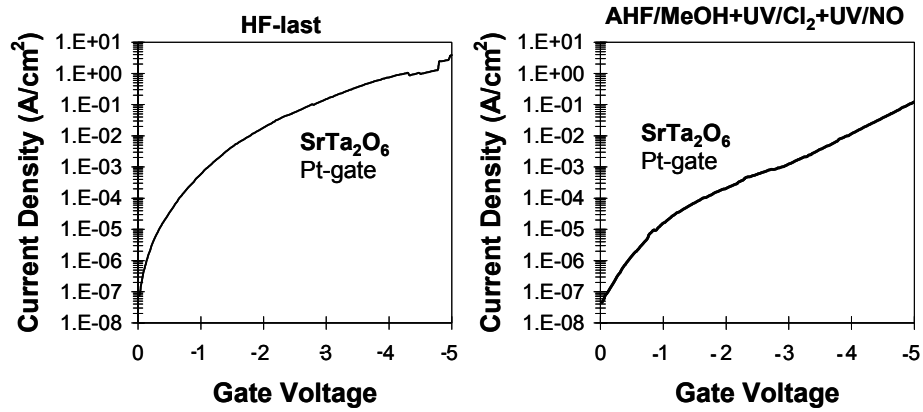


Fig.7 J-V characteristics of 5nm thick SrTa₂O₆

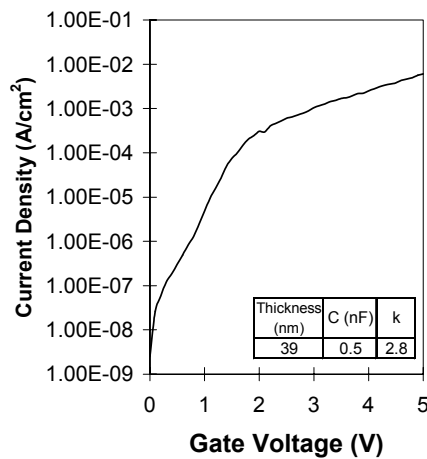


Fig.8 Electrical characteristics of Pyralin® PI2610