Studies of High-k Dielectrics Deposited by Liquid Source Misted Chemical Deposition in MOS Gate Structures

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Abstract

This paper reviews results of an investigation of electrical characteristics and selected fundamental material properties of several high-k metal oxides considered for MOS gate applications. The metal oxide films were deposited using the LSMCD (Liquid Source Misted Chemical Deposition) method in a cluster tool. The method produces high quality films as thin as 3 nm and offers the flexibility of switching between various chemistries. Among compositions studied mist-deposited oxides of Hf and Zr as well as $SrTa_2O_6$ were found to display promising characteristics for MOS gate applications with the last showing superior thermal stability with silicon.

Keywords

Liquid Source Misted Chemical Deposition (LSMCD), gate oxide, high-k dielectrics, equivalent oxide thickness

1. Introduction

For MOSFET and CMOS devices to work properly a certain minimum capacitance of the gate structure (Metal-Oxide-Semiconductor) is required. For years the decrease of gate capacitance resulting from the reduction of the gate contact area was compensated by gradual thinning of the silicon dioxide film in the MOS structure. There is a limit to this procedure, however, as at thicknesses of the gate oxide approaching about 1 nm the effectiveness of the MOS gate in controlling channel conductivity will be hampered by the tunneling current flowing between the gate contact and the silicon [1]. Consequently, in order to assure a sustained growth of CMOS technology in the sub-0.1 µm geometry range, the tunneling current in the MOS gate stack must be suppressed by using gate oxides in the 3-5 nm thickness range. In order to assure the required capacitance of the gate at the same time, the gate oxide used will have to feature a sufficiently high dielectric constant k. With its low dielectric constant (k=3.9) silicon dioxide, SiO_2, will no longer be used as a gate oxide. Assuming 3 $\mu F/cm^2$ (capacitance of an MOS gate with 1.0 nm thick SiO_2) as a minimum capacitance required, one can predict values of equivalent k (k of the gate dielectric stack, k_{eq}) needed for various thicknesses of the gate dielectric. As seen in Fig. 1 a gate dielectric system with k_{eq} 15 or higher will have to be processed on Si substrates to meet this required capacitance at 3 nm. If the gate dielectric would include only one material in direct contact with silicon then in order to assure equivalent oxide thickness EOT = 1.0 nm the k value of a 3 nm thick gate dielectric will have to be at least 15 (Fig. 2). However, in the case a slightly nitrided (k=4.5), 0.5 nm thick interfacial oxide would be present, then the gate dielectric would have to feature a k of at least 25. As seen in Fig. 1 and 2 requirements

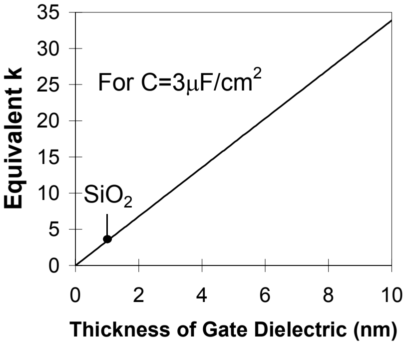

Figure 1: Thickness vs. equivalent k for $C=3\mu F/cm^2$

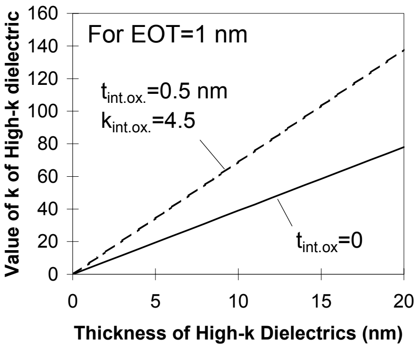

Figure 2: Thickness vs. value of high-k dielectrics for EOT=1nm

regarding the k value would be even more stringent when thicker gate dielectrics would be used.

The requirement regarding the value of k is only the first on the list of requirements alternative gate dielectrics must meet with low leakage current being the obvious other one. Also, thermodynamical stability of the gate dielectric with silicon which allows formation of gate dielectric-Si structures without oxidizing the Si surface, and hence, without uncontrolled formation of an interfacial SiO_x is expected. An interfacial oxide may actually be desired in the gate structure in order to passivate surface states and to assure adequate electron mobility in the MOSFET channel, but then an adequately higher k alternative dielectric will have to be used (Fig.2). Furthermore, it is important that the gate dielectric does not undergo structural/compositional transformations resulting in degradation of its characteristics during anneals following deposition. Moreover, the material should not display ferroelectric properties and should have characteristics independent of frequency. It is also important that the technology of the possible alternative gate dielectric, e.g. etching, cleaning, etc., will be compatible with standard Si manufacturing procedures. Several dielectrics are considered for advanced MOS gate applications (e.g.[2,3]). Among them, oxides and silicates of zirconium and hafnium appear to attract the greatest attention at present. Several other materials were extensively evaluated and then abandoned because of one or more deficiencies. Ta_2O_5 for instance was found to display insufficient thermal stability with silicon. The materials of interest are deposited using a variety of methods including Molecular Beam Epitaxy (MBE) and Atomic Layer Deposition (ALD) as well as CVD, sputtering, and jet vapor deposition.

In the reported investigation, gate dielectric films are deposited by means of the Liquid Source Misted Chemical Deposition (LSMCD) method [2]. The goal of this study was to investigate current-voltage, and capacitance-voltage characteristics of MOS capacitors incorporating LSMCD deposited dielectrics as well as selected fundamental material properties of several dielectrics including La_2O_3, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, $LaAlO_3$, $LaScO_3$, $ZrSiO_4$, $HfSiO_4$, $SrTiO_3$ and $SrTa_2O_6$. Based on the results of a preliminary evaluation oxides and silicates of zirconium and hafnium as well as $SrTa_2O_6$ were selected for more thorough characterization.

2. Experimental

The LSMCD technique employs liquid metal-organic precursors as a source. The liquid is atomized and deposited in a controlled amount in the form of sub-micron mist droplets onto the wafer surface at room temperature and atmospheric pressure. The process is carried out in a nitrogen ambient and a high-voltage electrostatic field is used to control the deposition rate.

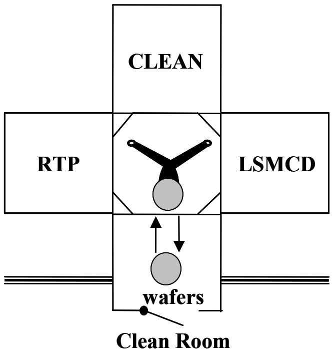

Figure 3: (a) Cluster tool used in this study

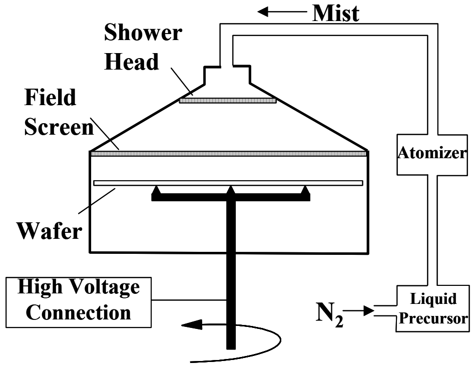

Figure 3: (b) Schematic diagram of LSMCD

In this study, the deposition runs were carried out in a commercial cluster [5] (Fig. 3a) consisting of a gas-phase surface conditioning module, a LSMCD module (Fig. 3b), and a Rapid Thermal Processing (RTP) module in which wafers are annealed after deposition at temperatures not exceeding 700 ^{o}C. The surface conditioning module allows etching of native/chemical oxide (anhydrous HF/methanol process), slight etching of silicon (UV/Cl_2 process), and regrowth of ultra-thin oxide using a UV/NO process.

P-type, (100) Si wafers 150 mm and 200 mm in diameter and with varied resistivity were used as substrates. In most cases prior to loading into the cluster wafers were subjected to a brief HF: H_2O (1:100) etch followed by a rinse-dry cycle and no additional surface conditioning was employed in the cluster. In some runs wafers directly out of the box were subjected to surface processing in the cluster and then transferred to the deposition module. Some wafers following deposition and an in-situ anneal in the RTP module (Fig.3a) were subjected to an additional anneal in a conventional furnace typically at 700 °C. Thicknesses of the films studied varied from 3 to 10 nm and were determined by means of ellipsometry as well as TEM. The AFM and SEM techniques were used to monitor surface morphology of the deposited materials.

Electrical characterization was carried out using MOS capacitors with e-beam evaporated Pt/Ti or Pt contacts. Most of the measurements were carried out using a contact area of either 3×10^{-4} cm^2 or 9×10^{-5} cm^2. Current density-voltage measurements were carried out and leakage current density was compared at V_g=-1V. Standard high frequency C-V measurements at either 100kHz or 1 MHz were performed to determine the density of capacitance in accumulation, equivalent oxide thickness, and other parameters of the high-k dielectric/Si structures.

3. Results and Discussion

During an early stage of this investigation the conductivity of various materials in an MOS structure was investigated. Figure 4 shows examples of current density-voltage characteristics of 9nm thick metal oxide films obtained in this study. The leakage current varied from material to material, but in no cases was an excessive leakage current observed. The current density was always less than 1mA/cm^2 at V_g=-1V, indicating highly adequate insulating properties of the LSMCD films. However, following thickness scaling to the sub-6 nm range followed by various tests carried out in conjunction with C-V characterization, it was determined [5] that some LSMCD-deposited materials (the same may not apply to the same compositions deposited using other methods) either do not pass the test from the manufacturability point of view, or the electrical properties point of view, or both. The materials that did show a very good promise included ZrO_2, HfO_2, $SrTa_2O_6$, $ZrSiO_4$, $HfSiO_4$, and Nb_2O_5. However, since our experimental results base for the first three compositions is the most complete, we focus our attention in this report on these three compounds. Good performance in MOS device structures was already reported for both ZrO_2 (e.g. [7,8]) and HfO_2 (e.g. [9]). This investigation did also demonstrate very promising electrical characteristics for LSMCD-deposited ZrO_2 and HfO_2. Figure 5 shows typical C-V characteristics obtained from MOS capacitors with mist-deposited ZrO_2 and HfO_2. As seen in this figure in both cases adequate behavior of the gate dielectric is observed. At V_G = -3 volts capacitance densities of about 2.5 µF/cm^2 and 3.3 µF/cm^2 for ZrO_2 and HfO_2, respectively, were obtained. The corresponding equivalent oxide thicknesses were 1.4 nm for ZrO_2 and 1.0 nm for HfO_2.

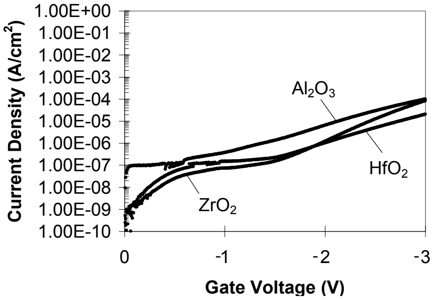

Figure 4: (a) Current density-voltage characteristics of 9nm thick binary metal oxides

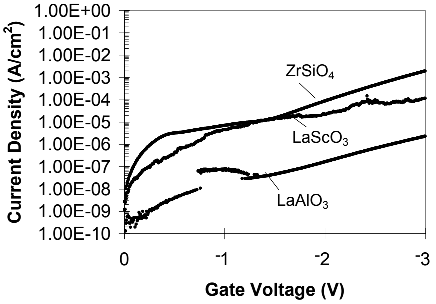

Figure 4: (b) Current density-voltage characteristics of 9nm thick ternary metal oxides

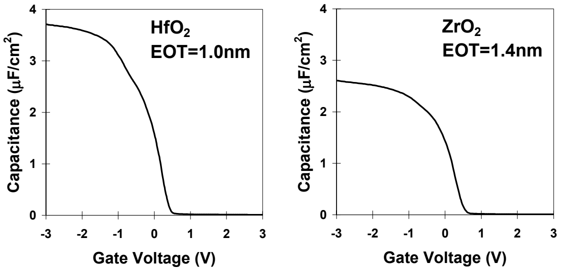

Figure 5: C-V characteristics of HfO_2 and ZrO_2

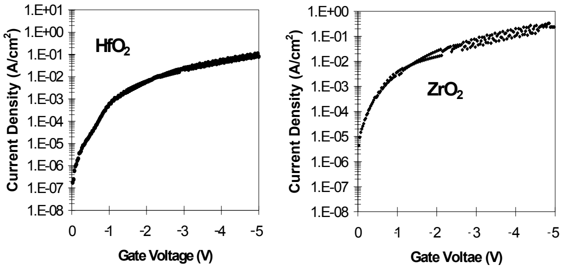

Figure 6: Current density-voltage characteristics of HfO$_2$ and ZrO$_2$

As J-V plots for the same devices shown in Fig. 6 indicate the leakage current at V_G = -1 volt in either case did not exceed 1 mA/cm^2. The k values could not be determined accurately based on the capacitance measurements as TEM characterization indicated the presence of two phases in the films: MSiO$_x$ at the Si surface and MO$_x$ comprising the "bulk" of the film (M = Zn, Hf). For the estimated thickness of the films of about 4nm the equivalent k (k_{eq}) values are estimated at about 12 and 15 for the dielectric structures resulting from the deposition of ZrO$_2$ and HfO$_2$, respectively. It should be noted that the presence of the MSiO$_x$ phase at the Si surface does not necessarily mean that the Hf and Zr oxides are not stable with Si. Possibly the interfacial silicates were formed during the post-deposition anneal carried out in the presence of oxygen.

The problem with LSMCD ZrO$_2$ and HfO$_2$ was that the promising electrical results obtained for these two materials occasionally did not display sufficient reproducibility suggesting possibly nonuniform coverage of the silicon surface with the Zr and Hf oxides in the thickness regime of about 5 nm and below. AFM and SEM characterization confirmed this notion showing local discontinuity of coverage observed regardless of the concentration of the precursor. Furthermore, the thermal stability of both these compounds was found insufficient. This was demonstrated by the degradation of electrical characteristics of ultra-thin films subjected to a 1 min. RTP process at 1000 ^{o}C in nitrogen. Similiar results were observed by other authors for instance in the case of sputter-deposited ultra-thin HfO$_2$ in which a phase transition takes place at 700 ^{o}C and higher [9].

As opposed to ZrO$_2$ and HfO$_2$ our early experiments did show excellent uniformity and smoothness of the Si surface coating with SrTa$_2$O$_6$ using the LSMCD method (Rms roughness in the 1 nm range). This particular material is difficult to synthesize and was not yet studied as an ultra-thin dielectric in MOS gates in spite of the fact that it seems to feature characteristics compatible with MOS gate requirements. The dielectric constant of the Sr-Ta-O system varies depending on the crystallographic structure and composition. For instance, single-crystal FZ grown SrTa$_2$O$_6$ has an anisotropic dielectric constant k=108 independent of frequency [9]. On the other hand, the Sr$_{0.85}$Ta$_{0.85}$O$_3$ perovskite phase crystallized on Pt-coated SiO$_2$/Si substrates from spin-coated films displayed k~16 [10]. Furthermore, SrTa$_2$O$_6$ is expected to display sufficient thermodynamical stability with the Si surface (Ta$_2$O$_x$ is not stable, but SrO$_x$ is stable) to limit uncontrolled growth of interfacial SiO$_x$. In this investigation a 5 nm thick film of SrTa$_2$O$_6$ did not show any degradation of capacitance or leakage current following a 1 min. anneal at 1000 ^{o}C in nitrogen.

Electrical characterization of LSMCD SrTa$_2$O$_6$ in MOS capacitor structures did produce very promising results. As seen in Figure 7 values of EOT in the range of 1 nm were obtained at the leakage current density in 10^{-6} A/cm^2 range.

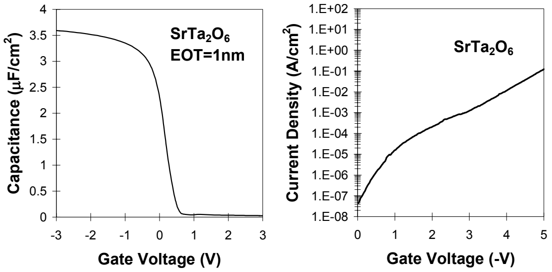

Figure 7: C-V and J-V characteristics for 5nm thick SrTa$_2$O$_6$

4. SUMMARY

The fundamental electrical and material characteristics of several high-k dielectrics deposited by the Liquid Source Misted Chemical Deposition (LSMCD) method were studied. The oxides of Hf and Zr as well as SrTa$_2$O$_6$ were studied in greater detail. The former two showed very adequate electrical characteristics but were lacking in terms of thermal stability and uniformity of coating using the misted deposition method. On the other hand, SrTa$_2$O$_6$ was found to display excellent coating characteristics, thermal stability with silicon and very promising electrical characteristics in MOS capacitor structures. Additional experiments are expected to shed additional light on this potential alternative dielectric for future generation MOS gate stacks.

References

[1]. C. Chang, C. Cheng, H. Lin, M. Liang, C. Chien, and T. Huang, Microelectronics Reliability, **39**, 553 (1999)

[2]. K.J. Hubbard and D.G. Schlom. J. Mater. Res., 11, 2757 (1996)

[3]. R.M. Wallace and G.D. Wilk, The Physics and Chemistry of SiO2 and the Si_siO2 Interface-4. Eds. H.Z. Massoud, I.J.R. Baumvol, M. Hirose and E.H. Poindexter, The Elctrochem. Soc. Proc Vol. 2000-2, 2000, p.465.

[4]. N. Solayappan, V. Joshi, A. Devilbiss, J. Bacon, J. Cuchiaro, L. McMillan, and C. Paz De Araujo, Integrated Ferroelectrics, 22, 1 (1998)

[5]. Technical Literature, Primaxx-2F™, Primaxx Inc., Allentown, PA

[6]. D.-O. Lee, P. Roman, P. Mumbauer, R. Grant, M. Horn, and J. Ruzyllo, Proc. Fifth Int. Symp. on Low and High Dielectric Constant Mat., The Electrochemical Society Proceedings Series, Pennington, NJ (2000).

[7]. Y. Ma, Y. Ono, L. Stecker, D.R. Evans, and S.T. Hsu, Intern. Electron. Dev. Meeting, IEDM 1999, p.149.

[8]. W.J. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banarjee, and J.C. Lee, Intern. Electron. Dev. Meeting, IEDM 1999, p.145.

[9]. B.H. Lee, L. Kang, W.J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J.C. Lee, Intern. Electron. Dev. Meeting, IEDM 1999, p. 133.

[10]. M.A. Rodriguez, T. J. Boyle, B.A. Hernandez, D.R.Tallant, K. Vanheusden, J. Am. Ceram. Soc, 82, 2101 (1999).

[11]. I. Tanaka, Y. Sato and H. Kojima, J. of Crystal Growth, 99, 837 (1990)